Low Power DPDT Switch Designed on VLSI

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ABSTRACT

In this paper it is designed DPDT switch by using two SPDT switches. In this it is further discussed about the basics of VLSI and the processing stepsalso. The MOS switch and the MOS inverters are also discussed to make the well understanding of switches. The designing of combinational circuits are discussed and DPDT switches basics are explained. Low power techniques and the methodologies as well as all low power concept are analysed. The lay out diagram which proposes the DPDT switches and matching with low power low voltage technology.

I.INTRODUCTION

VLSI- Very Large Integration Technology where millions of transistors which can be integrated on a single chip or single die. But these which have the combination of both analog and digital function. CMOS- Complementary MOS (Metal Oxide Semiconductor) has mixed signal implementation. It provides density and power savings on digital side and good mix components of analog design. CAD methodologies which have been successful in automating design of digital system.

IC'sare categorized into two major categories analog and digital. Analog signal whichis defined over continuous range of time and amplitudes. Digital signal is defined onlyat discrete values of amplitude. Analog sampled data signal is a signal that is defined over a continuous range of amplitude. But only at discrete points in time. Circuit design is the creative process of developing a circuit that solves a particular problem. Synthesis or design of a circuit is the process by which one starts with a designed set of properties and finds a circuit that satisfies them.

II. PROCESS STEPS

Oxidation, diffusion, ion implantation, deposition and exchange photolithography is the process of defining the area of the semiconductor subject to processing. There are

two methods of growing crystals on the silicon.

- Czochralski method Float zone
- technique

The process of exposing selective areas of a wafer to light through a photo maskwhich is called printing.

- Contact printing Proximing
- printingProjection printing
-

A circuit defined and functioned properly at the schematic level can fail it is not correctly designed physically. Physical design, which is referred to as layout.
Matching concepts to be followed. The rate for making two components electrically equivalent is simplified to draw them as identical units. This is the unit matching principle. Two components are identical mean that both they and their surroundings must be identical.

MOS transistor layoutResistor

- layout Capacitor layout Layout
- ruler
-
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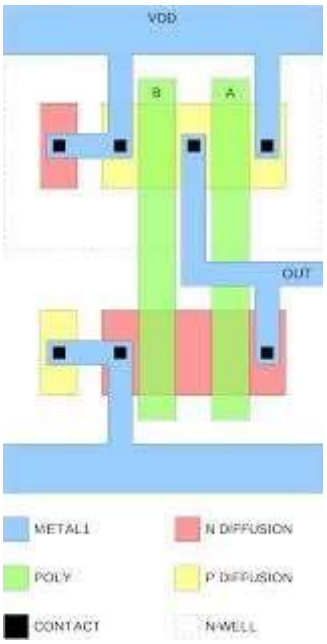
III. MOS SWITCH



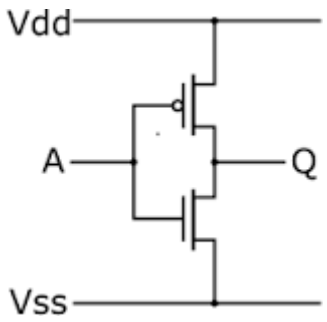
The switches which finds many applications in IC. The MOS switch which isused to implement many useful applications. The applications are multiplexing,

modulation are actually the switches are act as transmission gate in digital circuits. The study of characteristics of switches are compatible is CMOS IC. The parasitic capacitors are very important while considering the applications of analog sampled data circuit. The capacitors used here are very effective is called charge feed through. In this the portion of Vc. (i.e.) collector voltage appears at the switch terminals.

One advantage is that MOS technology is it acts as a good switch. One important aspect of the switch is range of voltages. This particular range of voltage which is compared to control voltage. The primary advantage of CMOS switch over the single channel MOS switch is that the dynamic analog signal range in the state is greatly increased.

IV. MOS INVERTERS

To design any logic circuits for complex range of devices inverter is in need. It is necessary for restoring logic levels for NAND, NOR gates, for sequential and memory circuits. IC consists of layers of insulating semi conducting and conducting region. These are layers which are assembled to form transistors. These are interconnected to produce a certain desired electrical function.



V.MINIATURIZING VLSI CIRCUITS

Miniaturization which involves the way in which individual transistor characteristics change as the dimension change. Feature size, device size which will be minimized. The dimension is a function of both the minimum dimension. The minimum dimension the lithographic process will allow is function and the limitation of lithographic tools.

VI.COMBINATIONAL CIRCUITS

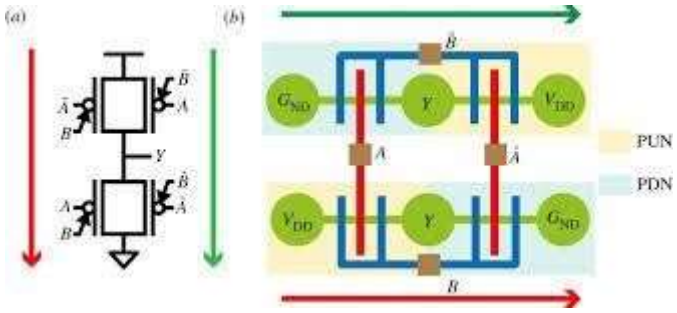
Designing a combinational circuit which is based on Static CMOS gate which is the combination of PUN and PDN.PUN which is PMOS gets connected with VDD and PDN which is connected to VSS which is NMOS. Here the input of be any one of the state which is conducting in steady state. These networks are actually named as Dual networks. These networks which provide

✓ High noise margin

- ✓ No static power consumption
- ✓ Comparable rise and fall times

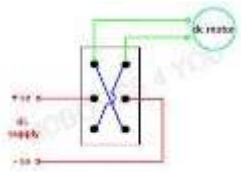
The performance which can be improved by using the techniques known as Progressive transistor sizing. As well as transistor ordering improved logic design anduse another circuit style. The static CMOS design has excellent speed, Low power consumption, Low sensitivity to noise, process variation.

Pass transistor logic is function where the change from one node of the circuit to another node under the control of the gate voltage. But the problem is Charge sharing and sneak path. Sources of power consumption in CMOS gates are switching activity, Glitching and direct path. Power is consumed only when switching of gates happened.



a) Block diagram, b) Lay out diagram

VII. DPDT SWITCH



DPDT switches which are actually two separate SPDT switches which are attached to same switch BAT. Thus SPDT is a toggle switch connects to a common terminal to one or the other two terminals.

VIII. LOW POWER CMOS

Transistors are the next generation of vacuum tubes. Vacuum tubes which consumes several hundred volts of anode voltage and few watts of power. But transistors required only mill watts of power. The next generation this is IC which has very less power dissipation. The battery powered application which is termed as low power

electronics- such as electronic calculators. Thus power requirement reduction is oneof the liable characteristics for microelectronics technology. There are three sources of power dissipation. The first is due to signal transitions, second comes from short circuit currents, and the third is due to leakage currents.

IX. CIRCUIT TECHNIQUES FOR LOW POWER

The total amount of power dissipation basically consists of static and dynamic. Many circuit techniques are proposed which reduces dissipated power in VLSI circuit design. Some techniques are optfor Static and Some techniques are opt for dynamic. In CMOS where dissipated power is due to logic transition. In switching activity logic transitions are predominant. Thus one way of influencing delay of a CMOS circuit changing W/ L ratio.

Stand by leakage control using transistors stack which is self-reverse bias.One of technic reduces sub threshold leakage current. Here more than one transistors stack is tured off. In the DPDT switches where two SPDT switches are connected together. Hence once the leakage current is reduced in such a way automatically the logic transitions also reduced. The total leakage current depends on the input applied.The random search based technics are used to find the input combination. Multiple threshold voltage technics are used to deal the leakage current with threshold voltage. The high threshold voltage sub threshold leakage current and low threshold voltage used to achieve high performance.

In this there are many technics where MOXCMOS circuit techniques used.It ismulti oxide CMOS circuit technic where gate oxide thickness which are used top modify the threshold voltage of the transistor.Thus the leakage current getting suppressed and performance also achieved.

X. LOW VOLTAGE, LOW POWER DESIGN TECHNICS

The main aim of VLSI designers are low voltage and low power for all the man-made circuits. Even though the power consumption is low the device speed should to be high. Thus the static and dynamic logic styles are used in which the static logic families to evaluates the output whenever there is an input variation. The dynamic logic gate where the output generated only once with each clock cycle.

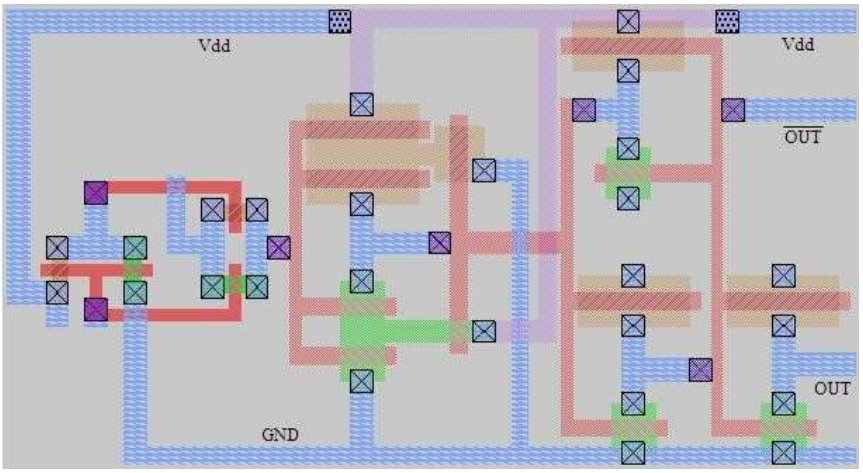
XI. POWER REDUCTION

There are many number of effective power reduction technic while designing the large and complex system. Power dissipation is the major bottle neck in large system design.Toreduce the average and peak power dissipation it is must to reduce the switching capacitance or reducing the supply voltage. Algorithm and architecture level transforms for low power which has two different technics. In the first technic uses differential co efficient representation to reduce the dynamic range computation. The 1's in co efficient representation which is reduced which optimizes the reduction in number of addition. To design the power supply network there are two options

which uses single network and supply different VDD at different time. In this work the first option is used. Because the will be dissipated too high while using different VDD. The through is one way, thusthe is presented. To manage the power dissipationand power management and many different schemes are used at each level of design abstracts.

XII. RESULT

The lay out diagram of DPDT switch which is shown under. By using the DPDT switch the input which is given and the output which is passed through. The output which is passed through by the switching action.



XIII. REFERENCES

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