A Nanoscale CMOS Technology for Hardened Latch with Efficient Design

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Abstract

CMOS technology scaling is mostly focused on high-performance and high- speed circuits, the potential use of advanced nanoscale technologies for ultra- low power (ULP) applications. The circuit reliability, delay, and energy consumption are among the most important issues that are affected by device variability. Radiation-induced soft errors threaten the robustness of logic circuits in nanoscale technologies due to reduced node capacitances and higher frequencies. This has led to the development of hardening techniques for soft- error resilient latches. The basis for the method of hardening is presented, where a storage cell called Dual Interlocked storage Cell (DICE) is introduced. An improved latch is designed based on the DICE cell is with improved SER robustness and minimal speed degradation. The circuit techniques for soft error tolerance can be made robust and be implemented relatively cheaply.

Keywords: Dual Interlocked storage Cell, NanoCMOS, SER, Soft error.

Introduction

Soft errors, which are transient errors caused due to external radiations, electromagnetic interface or electrical noise. Soft error rates (SER) in data-path structures and combinational logic have been increasing due to: Continuous device scaling, Voltage scaling and increased speed.

Three fundamental fault tolerance schemes 1.Hardware (spatial) redundancy: Assumption that defects and radiation particles will only hit on a specific device and not another device.2.Time (temporal) redundancy: Assumption that the radiation strike will not happen on the same circuitry against at a slightly later time.3.Information redundancy using error-detecting code or error-correcting code to

represent information.4.Hardening techniques. Now in modern technologies memory arrays are now well protected with interleaving of cells and Error Correction Codes (ECC), the Soft Error Rate (SER) in combinational and sequential logic. Modern technology scaling has made logic elements vulnerable to soft errors in three primary ways.

Previous Technologies

Generally a particle may hit logic gates, storage elements, or clock network of a digital circuit. When it hits the drain of transistors in logic gates, injects charge and causes a glitch in the output node voltage which is called single event transient. At theprocess level, silicon-on insulator (SOI) technology employs a buried insulating layer that limits the volume of bulk material available for generation and collection of ion- induced charge.

The rate at which soft errors occur is referred to as soft error rate (SER). Particle hits a control signal, such as the clock signal, it may generate a false control signal that can results in an unwanted data latch or timing violation. Memories are protected by Error Correction Codes (ECC). Due to continuous scaling trends, increased frequency and wide spectrum of particle energy, the probability that a transient voltage reaches storage elements in capturing window and gets latched, is increasing and so does the soft error rate. The spatial redundancy uses multiple copies of a given circuit with majority voting to determine correct outputs. Temporal redundancy technique is based on delayed sample of data, and is more suitable for conventional designs due to its lower power consumption. This technique can eliminate all SET pulses smaller than a certain threshold value.

Hardening Techniques

The dual interlock cell (DICE) is a soft error hardening circuit topology based on spatial redundancy. It consists of two p-device and n-device loops.

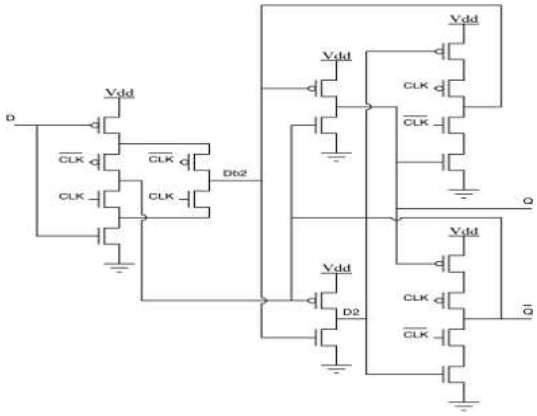


Figure 1: DICE using PMOS and NMOS

The basis for the method of hardening is presented a storage cell called Dual Interlocked storage Cell (DICE). The storage cell has four nodes for storing data each node is being controlled by two adjacent nodes, they do not directly depend on each other. Based on this idea, a conventional C^2MOS latch was modified to be soft-error resilient latch. Improved latch based on the DICE cell is presented with improved SER robustness in fig 2.

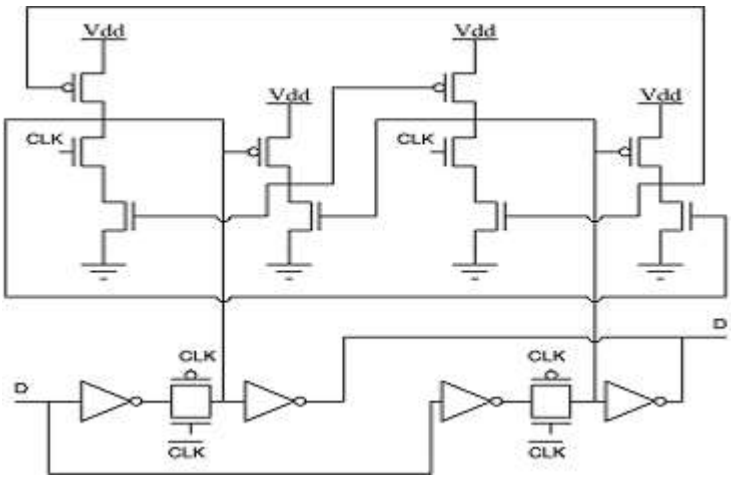


Figure 2: Improved DICE

The output node Q is connected to the two data nodes through inverters, allowing an extra stage of attenuation between the output and the soft-error sensitive internal nodes. However, because the final output effectively shorts the two intermediate data nodes, careful delay matching must be done in layout to prevent glitches at the output.

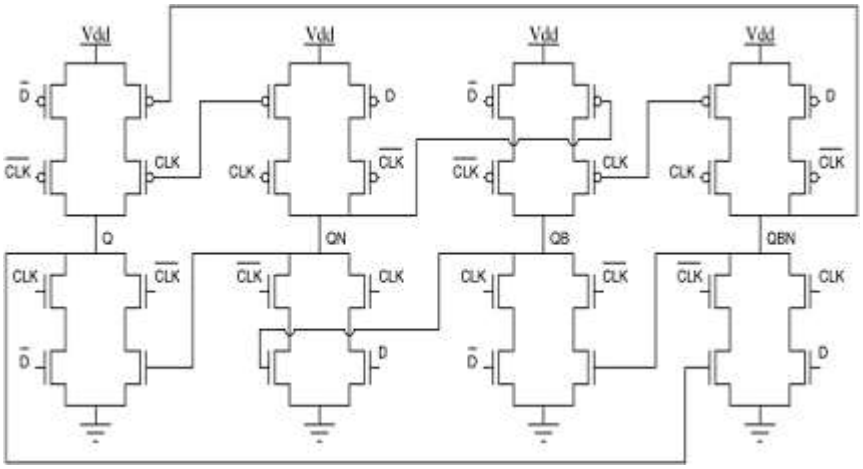


Figure 3: Proposed latch topology.

To overcome the problem of asymmetrical delays from dual data storage nodes to the output proposed another latch topology utilizing four nodes to store the data as shown in fig 3.If a glitch caused at any node feedback loop will force it back to its previous state. Due to the PMOS stacks low speed and high power consumption.

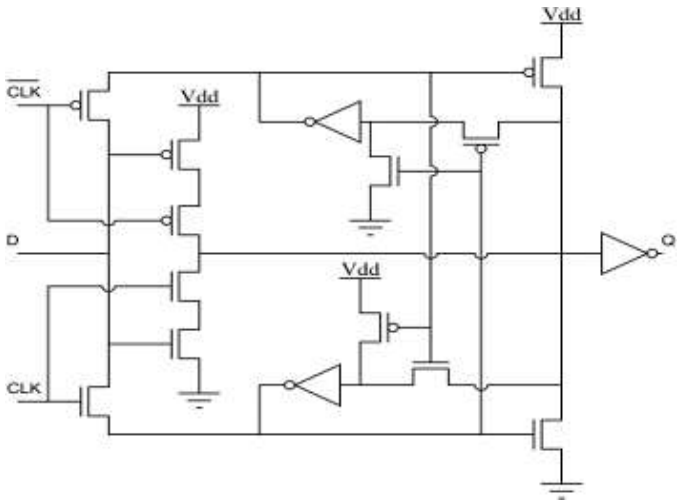
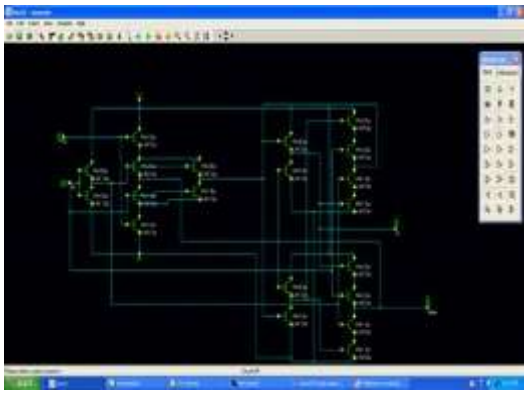


Figure 4: Improved Hardening Latch

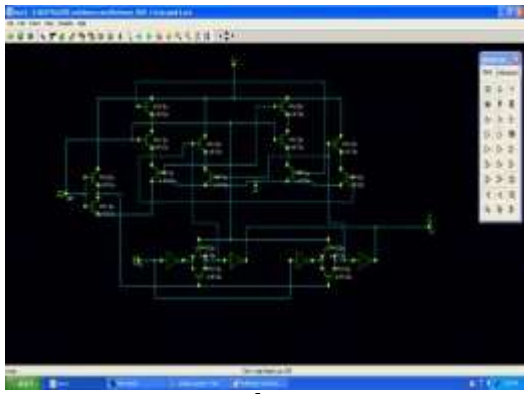
In Improved Hardening Latch three nodes are connected by a feedback structure so that an single event upset at the output node would always be driven back to the correct output by the alternate nodes. So that Single event upset at an alternate node does not affect the output node. We can get speed and can achieve low powerconsumptions.

Simulation Setup

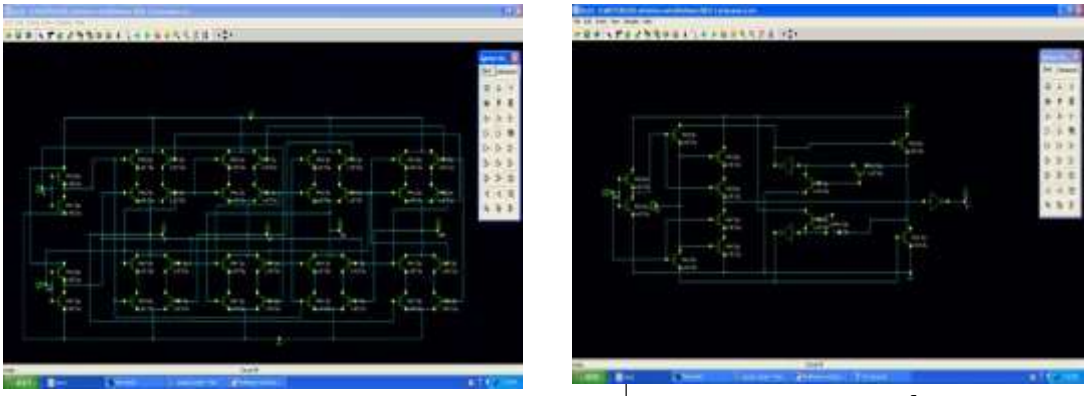
We used the Micro wind 3.5 to create and simulate the four latches. The outputs aremeasured. Power is measured by comparison with a minimally sized standard latch.



a



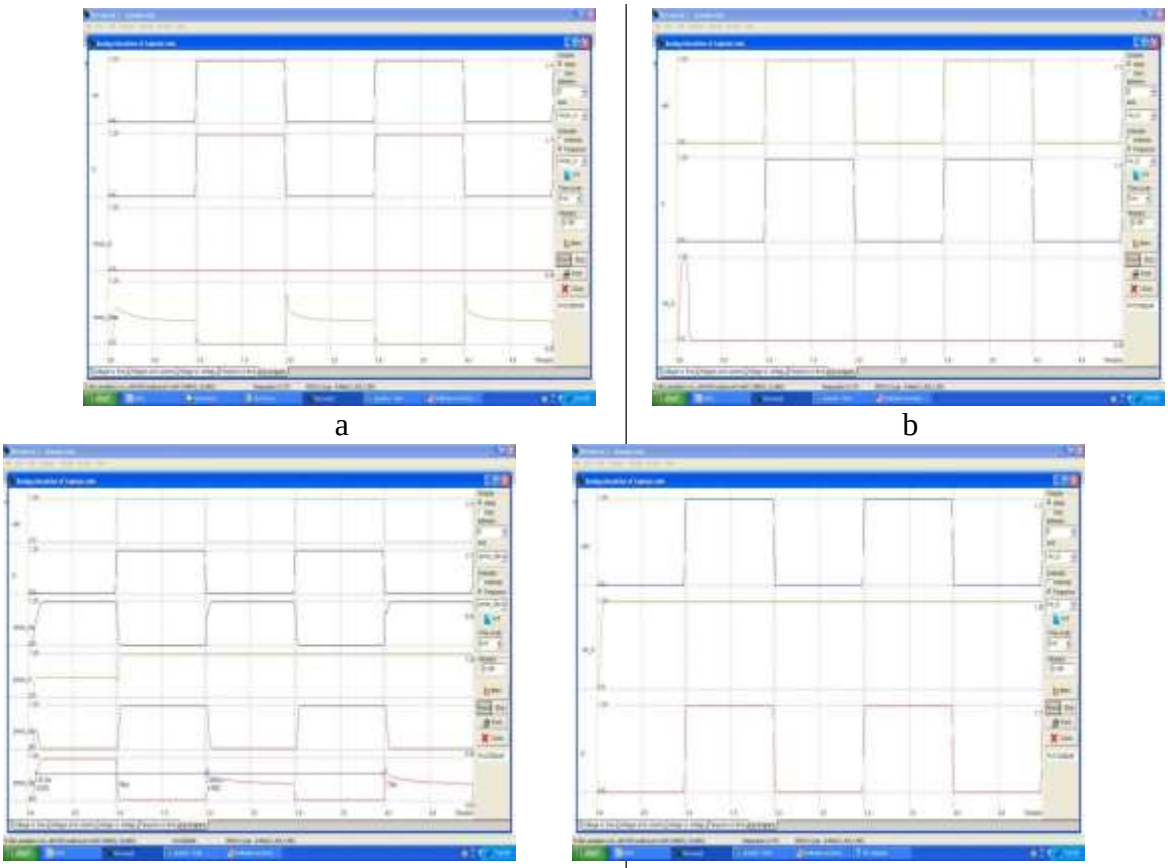
b



c d

Figure 5: a), b), c), and d) are the schematic diagrams of the four hardening latches.

Simulated Results



a b

c d

Figure 6: a), b), c) and d) are simulated results for latches in microwind tool.

Conclusion

This paper has presented new designs for hardening latch circuits in nano-scale CMOS and the problem of soft error tolerance in CMOS logic circuits was addressed.Novel configurations for latches have been proposed, analyzed, and simulated using the predictive technology microwind3.5 for tolerance to soft errors.We thus compared multiple latch hardening designs under controlled simulation conditions for low power consumptions. The Improved Hardening latch was found to be the most suitable for modern technology nodes because of its speed and low power. Apart from voltage scaling in modern circuits, there is a demand for increased clock frequencies and timing. So, built-in-resilience circuits will be more useful for future applications.

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