Power efficient offset compensated Track and Hold circuit Using Transmission gate based boot strapping

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ABSTRACT:

Different sample and hold (S/H) circuits are introduced, analyzed and simulated in this paper. It aims to illustrate the suitable sample and hold (S/H) circuit technique that is used in low voltage operation.Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. Different sample and hold (S/H) circuits are introduced, analyzed and simulated in this paper. It aims to illustrate the suitable sample and hold (S/H) circuit technique that is used in low voltage operation. All Clocked fully differential schemes are less sensitive to charge injection and other errors than conventional offset compensation schemes. Final proposed Ultra-Low-Power transmission gate based boot strapping method is proposed for efficient implementation of sample and holding circuit.

KEYWORDS: Track and Hold circuit, low power consumption, switched-capacitor filters ,low chip area, sampling switch.Clocked fully differential schemes, Transmission Gate, based boot strapping

INTRODUCTION:

ADC plays a vital role in component for Digital Signal Processor because most signals in the natural world such as voltage, current, and voice are analog. Sample and Hold circuits are required in front of high speed ADCs to improve their performance. Also its CMOS implementation is very important because of its low cost and single-chip integration of analog and digital parts is possible. We have designed a high-speed CMOS S/H circuit. High-speed S/H circuits for low voltage operation have already been implemented with BiCMOS and bipolar technologies. . Its use allows most dynamic errors of A/D converters to be reduced, especially those showing up when using high frequency input signals. Track and hold circuit is inserted in front of a comparator array of a flash A/D converter to keep comparator's input voltages constant while the comparators are settling their output voltage levels. At the circuit level in the low voltage operation. If the sum of the absolute value of the PMOS threshold voltage and that of the NMOS is greater than the supply voltage. The conventional analogue

switches consist of transmission gates may not be fully turned on as they are under a higher voltage operation. The MOSFETs expected to be turned on may have extremely poor conductance and would limit the bandwidth of the circuits. Therefore, a bootstrapped technique is required which has been proved . This Project includes different approaches for track and hold circuit. This paper investigates effect of various design schemes and circuit topology for track-and-hold circuit to achieve acceptable linearly, high slew rate, low power consumption and low noise. Superior speed & acceptable linearity of source-followers makes it promising candidate for the purpose of this work.

LITERATURE REVIEW From the rigorous review of related work and published literature it is observed that many researchers have designed different techniques for high speed communication in different techonologies. Since the real world today VLSI/CMOS very much in demand, from the careful study of reported work it is observed that track and hold circuit is the fundamental block for block for A to D converters. Its used for most dynamic errors of A to D converters to be reduced especially high frequency input signal. A.N. Karanicolas, "A 2.7-V 300-MS/s track-and-hold amplifier," IEEE J. Solid-State Circuits, Dec,1997. In this Paper A.N. Karanicolas invented a fully differential bipolar track and hold amplifier(THA) employed an openloop linearization technique compatible with low supply voltage. A feed through reduction method utilized the junction capacitance of a replica switch to provide a close match to the junction capacitance of the main switch.[1] W. Yu, S. Sen and B. H. Leung, "Distortion Analysis of MOS Track-and-Hold Sampling Mixers Using TimeVaryingVolterraSeries",IEEE Transactions on circuits and systems-II: Analog and Digital Signal Processing, vol. 46, No. 2, Feb.1999. In this paper time-varying theory of Volterra series is developed and applied in the sampleddata domain to solve for harmonic and intermodulation distortion of a MOS-based track-and-hold sampling mixer with a nonzero fall-time LO waveform. Distortion due to sampling error is also calculated. These results, when combined with the continuous-time solution, quantify harmonic and intermodulation distortion of a track-andhold type mixer completely. Closed form solutions are obtained. As a practical consequence, it is shown that for certain fall-time, the distortion of track-and-hold mixers can be better than what would be predicted by a simple application of time-invariant Volterra series theory.[2] A. Boni, A. Pierazzi, and C. Morandi, "A 10-b 185- MS/s track-and-hold in 0.35-µm CMOS,"IEEE J. SolidStateCircuits,,Feb. 2001. This master paper described the design of a track-and-hold (T&H) circuit with 10bit resolution, 185MS/s. It is designed in a 0.35µm CMOS process. The circuit is supposed to work together with a 10bit pipelined analog to digital converter.[3] Mohammad Hekmat and VikramGarg, "Design and Analysis of a Source-Follower Track-and-Hold Circuit", EE315 (VLSI data conversion circuits), June 2006, this paper investigates effect of various design schemes and circuit topology for track and-hold circuit to achieve acceptable linearly, high slew rate, low power consumption and low noise.[4] TakahideSATO†a), Member, Isamu MATSUMOTO, Nonmember,Shigetaka TAKAGI, Member, and Nobuo FUJII, Fellow, "Design of Low Power Track and Hold Circuit Based on Two Stage Structure",june 2008. In this paper, two track and hold circuits are designed and implemented using

65 nm CMOS technology. The first circuit is based on a dummy switch topology to decrease the charge injection error. The second circuit used a clock linearization technique to reduce the sampling instant inaccuracy. Simulation results showed that the track and hold circuit based on dummy transistor technique presented the best performances in terms of rapidity and accuracy.[5]

SAMPLE AND HOLD CIRCUIT:

A Sample and Hold Circuit, sometimes represented as S/H Circuit or S & H Circuit, is usually used with an Analog to Digital Converter to sample the input analog signal and hold the sampled signal. In the S/H Circuit, the analog signal is sampled for a short interval of time, usually in the range of 10µS to 1µS. After this, the sampled value is hold until the arrival of next input signal to be sampled. The duration for holding the sample will be usually between few milliseconds to few seconds.
The following image shows a simple block diagram of a typical Sample and Hold Circuit.

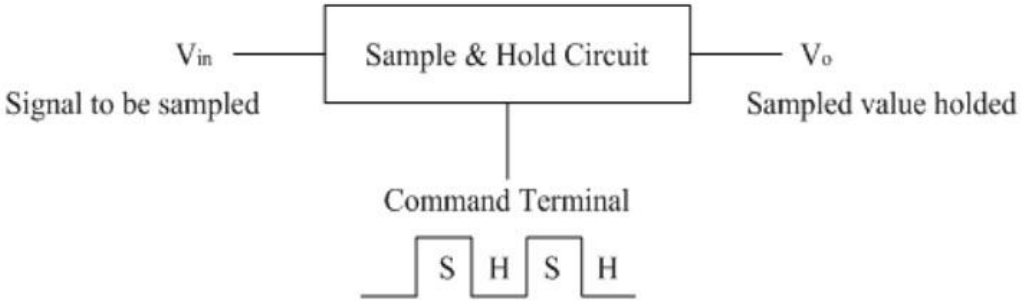

Fig1: General sample and hold

Need for Sample and Hold Circuits

If the input analog voltage of an ADC changes more than ±1/2 LSB, then there is a severe chance that the output digital value is an error. For the ADC to produce accurate results, the input analog voltage should be held constant for the duration of the conversion. As the name suggests, a S/H Circuit samples the input analog signal based on a sampling command and holds the output value at its output until the next sampling command is arrived.

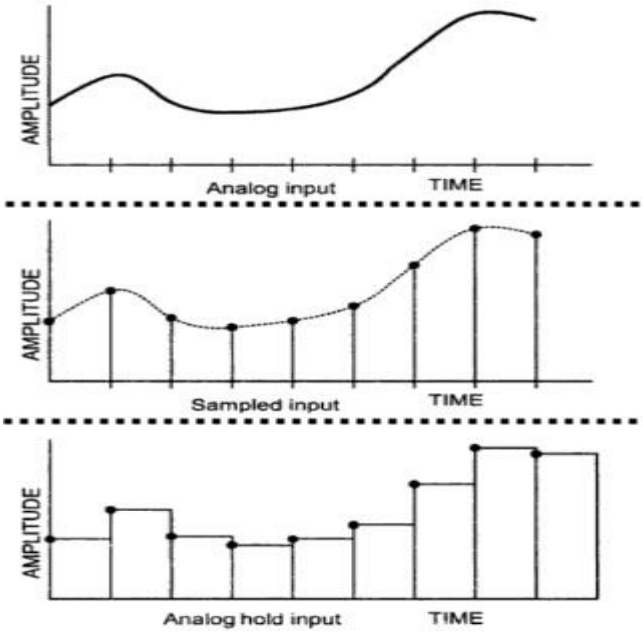

Fig2:Input and output waves of S&H

Let us understand the operating principle of a S/H Circuit with the help of a simplified circuit diagram. This sample and hold circuit consist of two basic components:

- Analog Switch
- Holding Capacitor

Figure1 circuit tracks the input analog signal as shown in figure2 until the sample command is changed to hold command. After the hold command, the capacitor holds the analog voltage during the analog to digital conversion.

OFFSET COMPENSATED MILLER T/H:

The track and hold (T/H) circuit of Fig. 3 is a modified version of the circuit of Fig. 2 that is able to compensate offset by storing its amplified version. This is done in order to make offset compensation less sensitive to charge injection and to other errors. A differential input stage (*Aoc*1) and an auxiliary differential output stage (*Aoc*2) have been added in order to store an amplified version of the total offset voltage. The outputs of three input stages (terminals A and B) are connected in parallel. Fig. 3c shows the transistor level schematic of the proposed T/H. The auxiliary input stage (*Aoc*1) is formed by transistorsMn3, and Mn3' while the auxiliary output stage (*Aoc*2) is formed by Mocp, Mocn, Mocp', and Mocn'. The proposed circuit works as follows:

1) During the hold phase _*H*, switches S3, S3', S5, and S5', are closed (Fig. 4a). This connects the inputs of the

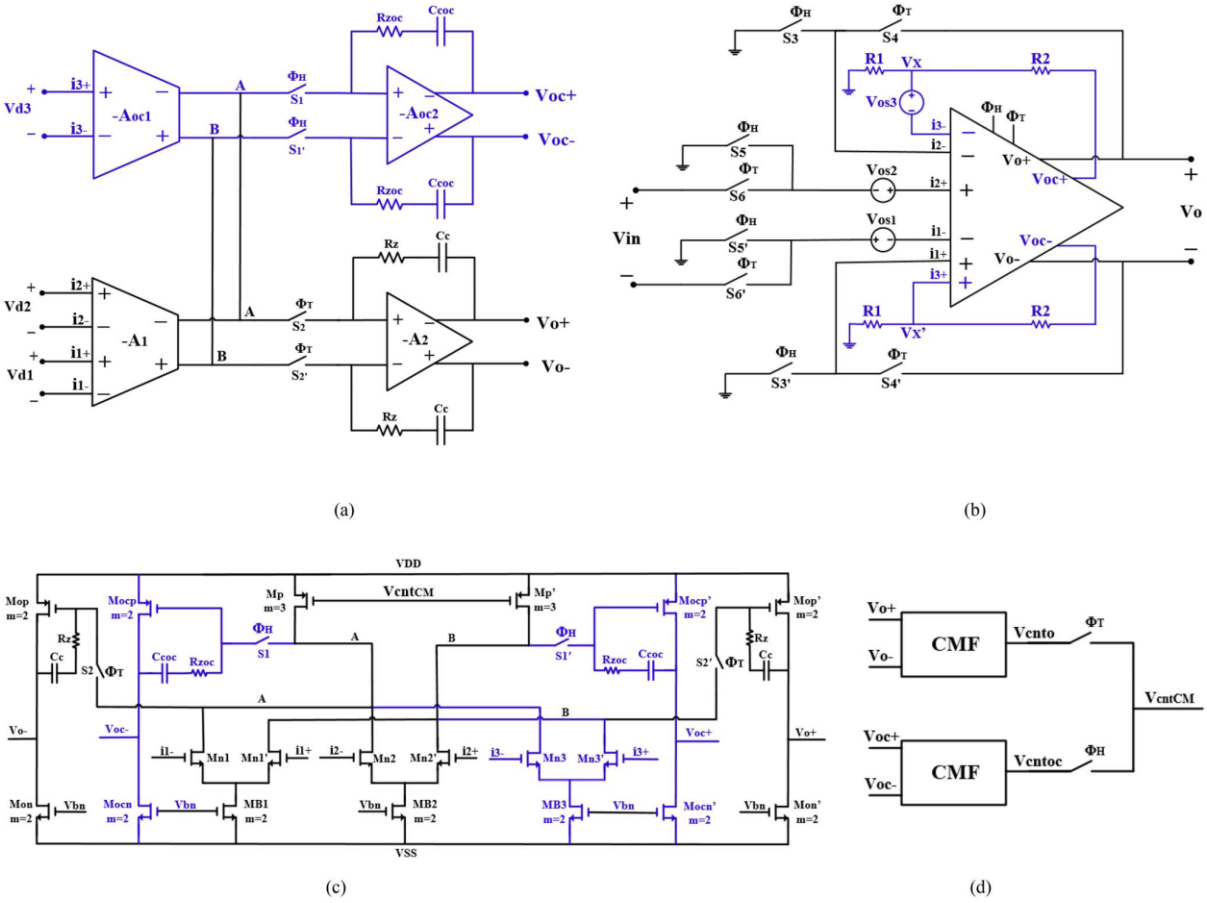

Fig. 3.Clocked fully differential offset compensation T/H. (a): Internal structure. (b): Voltage follower configuration. (c): Transistor level schematic. (d): Implementation of CMF in FD T/H.

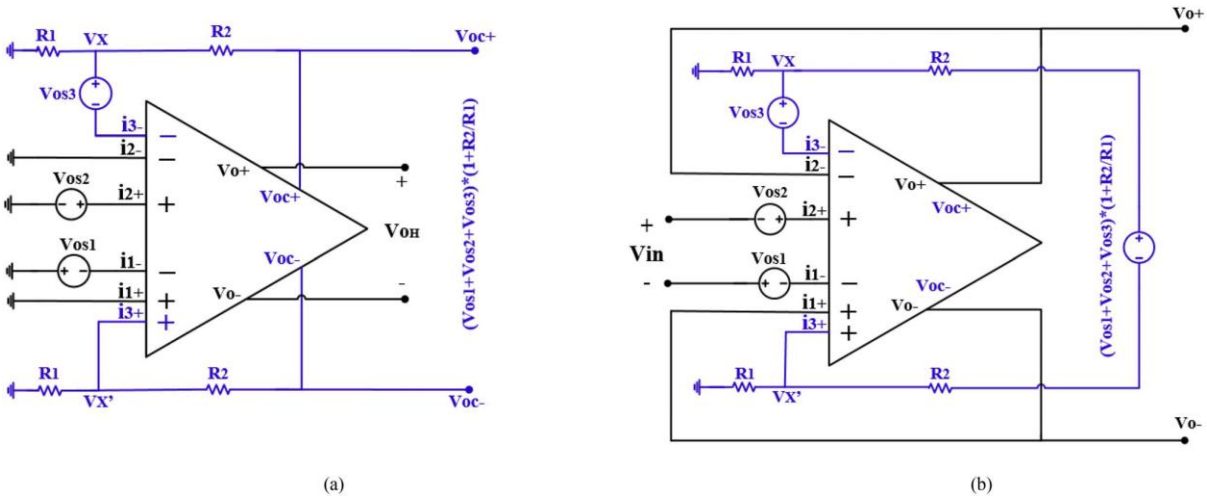

Fig. 4.Proposed T/H circuit including offset voltages. (a): During hold phase *_H*. (b): During track phase *_T* .

main amplifier to ground while the auxiliary amplifier implements an amplifier with gain *Goc*= 1+*R*2/*R*1. Its output voltage is given by *Voc*= *(*1 + *R*2/*R*1*)(Vos*1 + *Vos*2 + *Vos*3*)*.

2) During the track phase the main amplifier is connected as a FD buffer and the amplified offset *Voc*is held by the compensation capacitors *Ccoc*(Fig. 3b). In this case *Voc*performs as a DC voltage source that generates a voltage $VX - VX' = Vos1 + Vos2 + Vos3$ at the input of the auxiliary amplifier. This compensates the offset of all input stages and leads to an offset free main amplifier output *Vo*= *Vin*.

TRANSMISSION GATE BASED BOOT STRAPPING:

The multiplier circuit consists of M1, M2, C1 and C2. In below Figure, the gate of the NMOS transistor M3 which is responsible for charging the capacitor C3 is biased by the multiplier circuit. On the other hand, in below Fig, the NMOS transistor M3 is replaced by a PMOS transistor M3 and its gate is biased by the gate of the bootstrapped switch. M3 will charge C3 to (VDD) in the off-sate of the bootstrapped switch while in the on-state, the stored charge in C3 will be applied to the gate-source of the bootstrapped switch. Both circuits make the gate-source voltage of the bootstrapped switch constant and equal to the supply voltage independent of the input signal. This result in small and constant resistance of the sampling switch. The main important feature of the proposed modified low-power bootstrapped circuit is power consumption. It consumes less amount of power compared to the other presented bootstrapped S/H circuit in medium and high-frequency applications. In addition to that, the SNDR will not have degradation even in the high-frequency application.

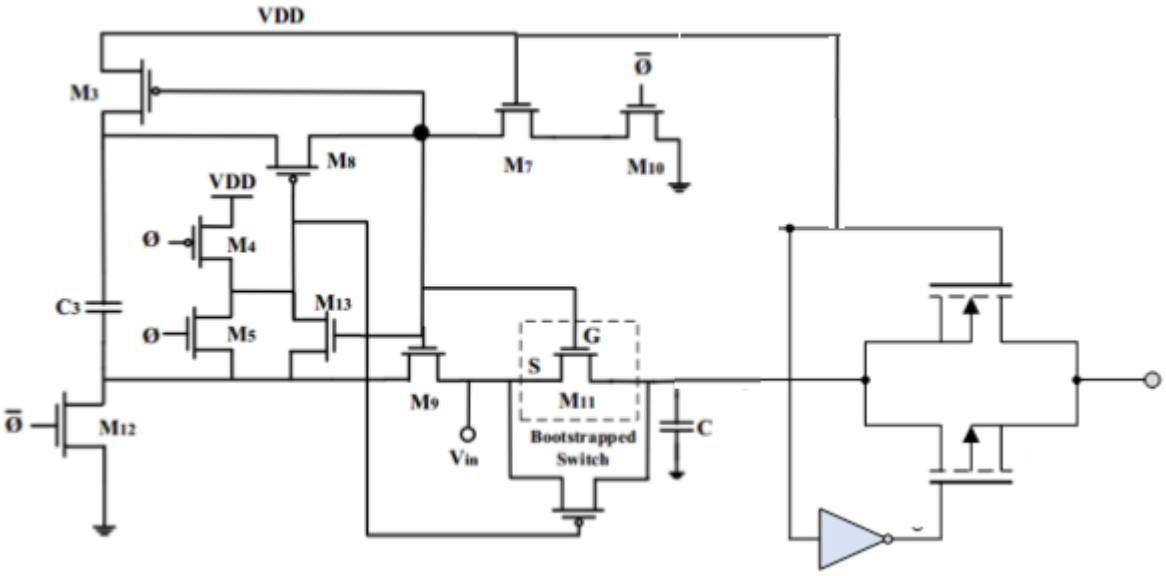

Fig5: Low-power bootstrapped S/H circuit without multiplier circuit.

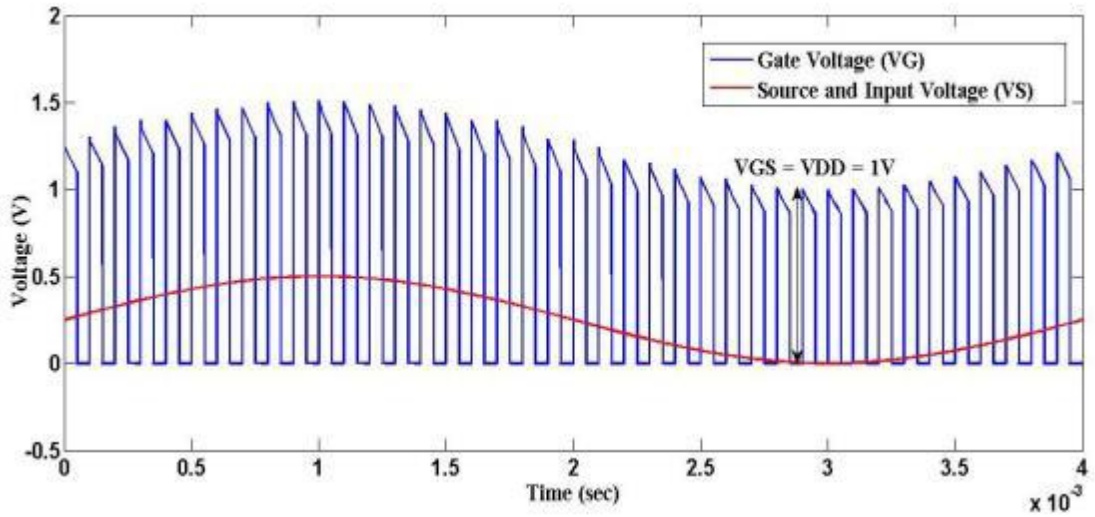

Fig6: Input signal with the clock pulses formed on G for the low-power bootstrapped S/H circuit without multiplier circuit.

RESULT:

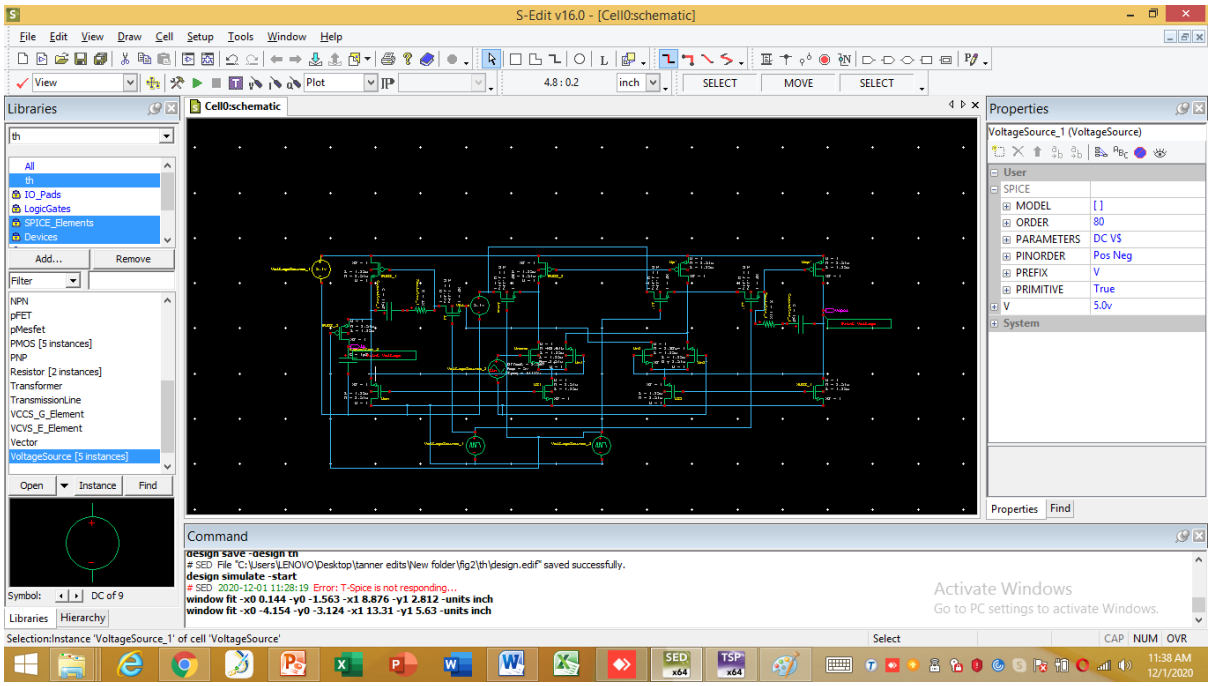

Fig7 : schematic of clocked fully differential circuit

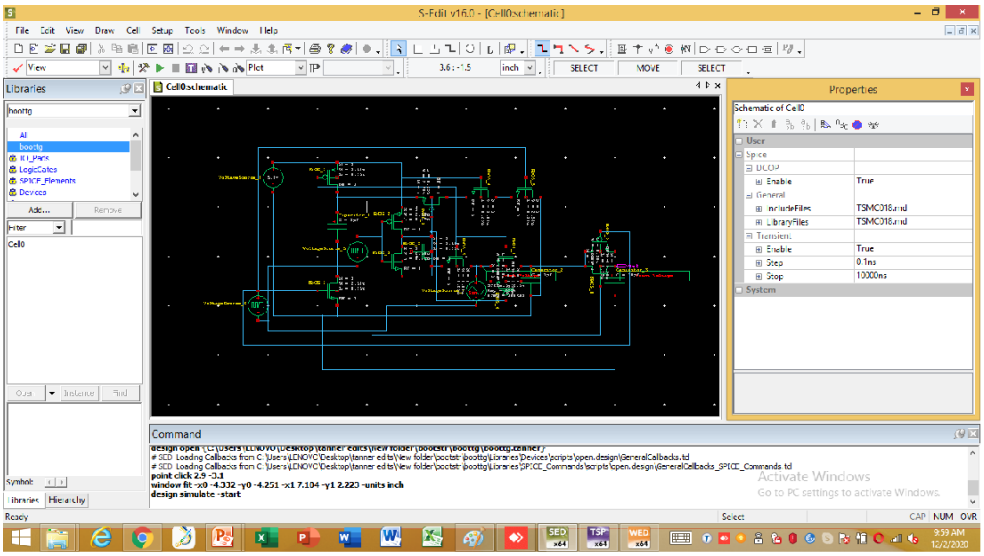

Fig 8 : Transmission gate based bootstrapping track and hold circuit

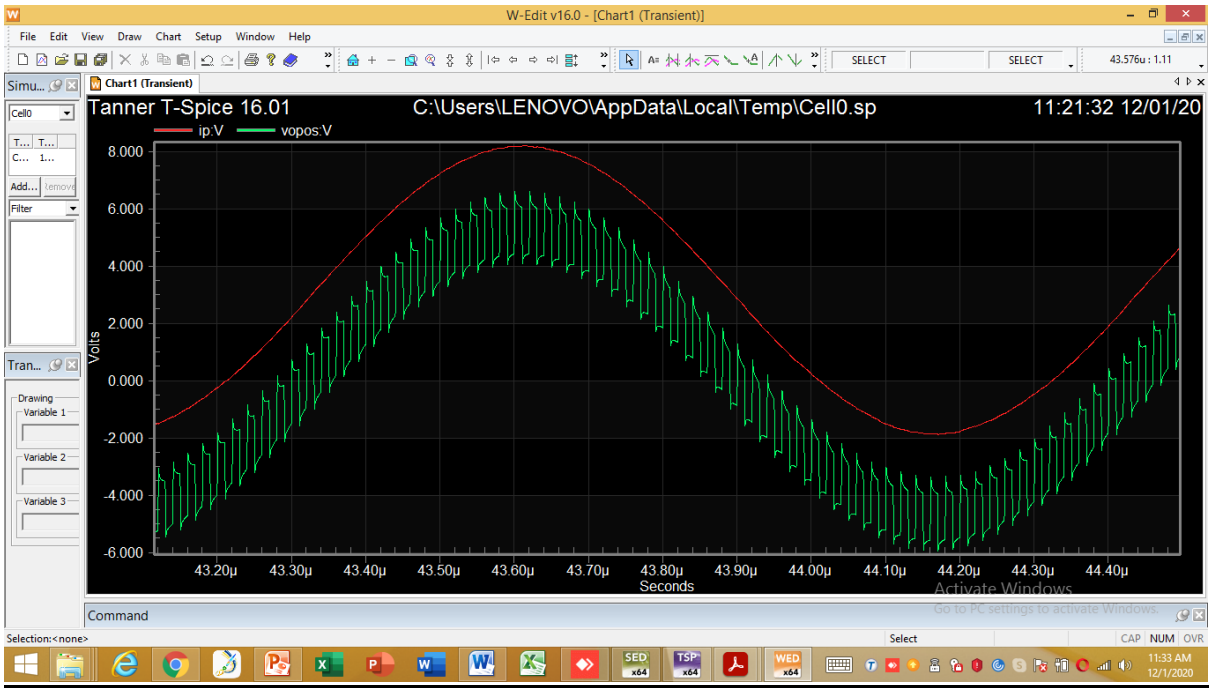

Fig 9 : waveform of fully differential track and hold circuit

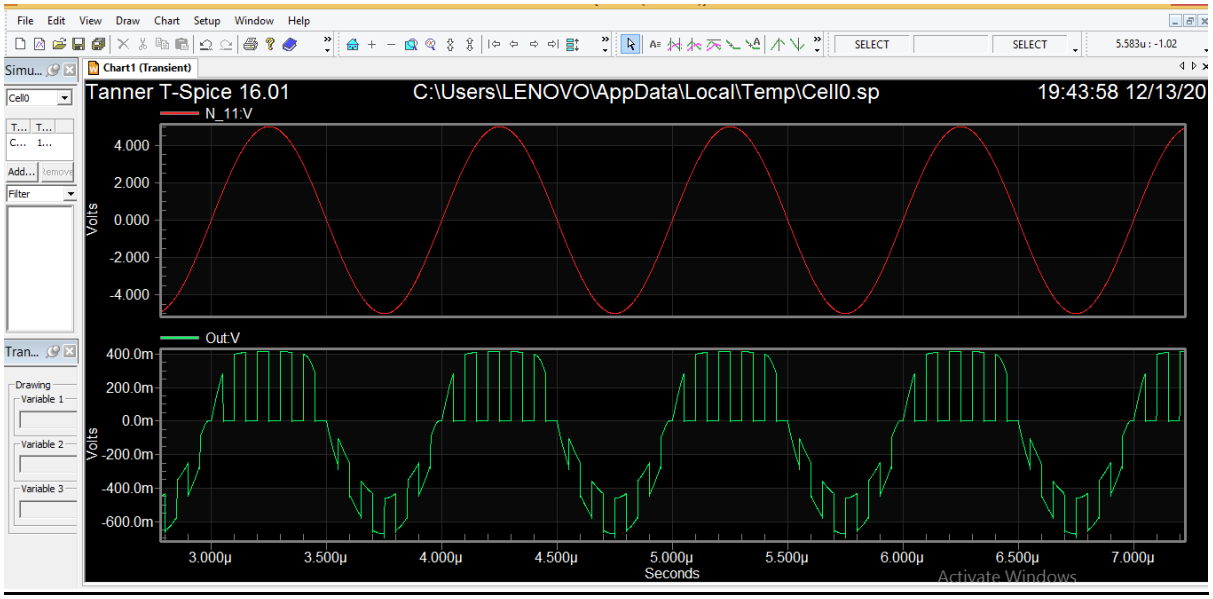

Fig 10 : output waveform of Transmission gate based boot strapping trackand hold circuit

CONCLUSION

Being a part of the ADC sample and hold is consuming high power. For low power consumption, Various sample and hold circuits like Bootstrap Circuit, Low-Power Bootstrapped S/H Circuit without Multiplier Circuit & clocked differential circuits are presented for better performance and low power consumption at different frequency applications . Finally In this paper the design of Clocked fully differential offset compensation T/H and TG based bootstrapped methodsare presented with detailed design calculations. Fully accurate zero DC offset output sample is obtained with more reliable.

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