Fault Port Method for Fault Analysis

Krishnapriya B, Assistant Professor, Department of Electrical Engineering, Krupajal Engineering College, Bhubaneswar
Subhendu Sahoo, Assistant Professor, Department of Electrical Engineering, NM Institute Of Engineering & Tech, Bhubaneswar
Soumyashree Sahoo, UG Student, Department of Electrical Engineering, Krupajal Engineering College, Bhubaneswar
Siddharth Mohanty, UG Student, Department of Electrical Engineering, Krupajal Engineering College, Bhubaneswar

***Abstract*- Faults are the basic hurdle for any power system network. As the complexities of the system increased, the probability of the occurrence of the fault also increased. Hence it is always better to take precautions which involve study of system under various fault conditions. This paper describes the generalized method for solving any combination of simultaneous balanced and unbalanced faults and calculating symmetrical fault port currents. This method can be applicable irrespective of any combination of faults, any number of faults and their location.**

Keywords—Simultaneous faults, fault port voltage, fault port current

I. INTRODUCTION

Load flow analysis requires the calculation of voltages and currents of all buses. These values assist in the control and planning of the system. Simultaneous faults are those cases in which there are one or more faults occurring simultaneously. The reason for the occurrence of such faults may be due to lightening stroke, human made accidents etc. and it is quite difficult to analyze more than one fault occurring at the same time. Faults mainly occur in sequentially rather than simultaneously. Keeping the aspect of protection in mind it is desirable to compute the voltage and current during and after the occurrence of first and second fault. For accomplishing this, system has to be monitored under all kinds of faulted situations. There are different types of faults which may be categorized as balanced and unbalanced faults. These simultaneous faults may be any combination of these balanced and unbalanced faults. Balanced faults can be of both symmetrical or unsymmetrical mode. [1].

An important method of simultaneous fault analysis comes from G. Gross and H.W. Hong in 1982 in the form of two-step compensation method [2], [3]. Papers [4], [5] and [6] deals with various other methods that could be adopted for simultaneous fault analysis.

This paper is based on the method of multiple port theory and theory of symmetrical components given in [4]. Current and voltage constraints for various fault types with reference to symmetrical components are shown in table I [7].

Under the normal fault analysis condition analyzing occurrence of fault on any phase is not a difficult problem but in case of simultaneous faults occurrence of faults on different phases has to be considered. Usually, mutual coupling is present between the lines but that is not considered in this paper.

The impedance matrix is to be modified whenever a fault occurs in a system. This is the mandatory requirement while doing fault analysis.. This modification can be anything ranging from addition or deletion of a bus as given in [8]. The sequence network interconnections are also another important point that needs consideration [7].

II. SEQUENCE NETWORK INTERCONNECTION

The interconnection between the sequence networks must be such that that all the limitations and the boundary conditions for that particular fault must be fulfilled. From table II it can be seen that for some faults the currents of all sequence networks at the fault point are equal and the sum of the voltages of all sequence network is zero from which we can conclude that the sequence networks are connected in series with each other. Similarly, for other types of faults voltages of all sequence networks are equal and the sum of all the sequence currents is equal to zero from which we can conclude that the sequence networks are connected in parallel.

In case of simultaneous faults it is not as simple as in case of single fault analysis. In very few combinations of faults these networks fulfill the connection constraints.

This difficulty mainly arises due to the occurrence of faults on different phases. To overcome this problem Z. X. Han has recommended using phase shifting transformers to shift the voltages and currents accordingly in order to meet the boundary conditions [4]. Ideal turns ration is given as:

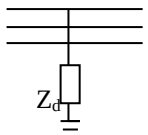
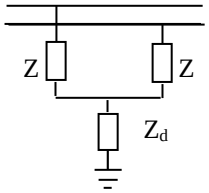
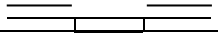
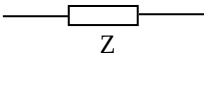
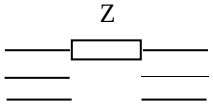
$$K = \frac{I1}{I2} = \frac{V2}{V1} \qquad (1)$$

where I1 and V1 are the primary current and voltage respectively of ideal phase shifting transformer and I2 and V2 are secondary current and voltage of ideal phase shifting transformer.

TABLE I. CONSTRINTS BETWEEN SYMMETRICAL CURRENTS AND VOLTAGES FOR DIFFERENT FAULTS

S.No	Fault	Current Constraints	Voltage Constraints
1	Single Line to Ground Fault	$I_1=I_2=I_0$ $I_1=a^2 I_2=aI_0$ $I_1=aI_2=a^2 I_0$	$V_1+V_2+V_0=0$ $V_1+a^2 V_2+aV_0=0$ $V_1+aV_2+a^2 V_0=0$
2	Line to Line Fault	$I_1= -I_2$, $I_0 = 0$ $I_1= - a^2 I_2$, $I_0 = 0$ $I_1= - aI_2$, $I_0 = 0$	$V_1 = V_2$ $V_1 = a^2 V_2$ $V_1 = aV_2$
3	Double Line to Ground Fault	$I_1+I_2+I_0=0$ $I_1+a^2 I_2+aI_0=0$ $I_1+aI_2+a^2 I_0=0$	$V_1=V_2=V_0$ $V_1=a^2 V_2=aV_0$ $V_1=aV_2=a^2 V_0$
4	Single Phase Open Fault	$I_1+I_2+I_0=0$ $I_1+a^2 I_2+aI_0=0$ $I_1+aI_2+a^2 I_0=0$	$V_{s1}=V_{s2}=V_{s0}$ $V_{s1}=a^2Vs_2=aV_{s0}$ $V_{s1}=aV_{s2}=a^2 V_{s0}$
5	Two Phase Open Fault	$I_1=I_2=I_0$ $I_1=a^2 I_2=aI_0$ $I_1=aI_2=a^2 I_0$	$V_{s1}+V_{s2}+V_{s0}=0$ $V_{s1}+a^2Vs_2+aV_{s0}=0$ $V_{s1}+aV_{s2}+a^2V_{s0}=0$

TABLE II. BOUNDARY CONDITIONS FOR DIFFERENT TYPES OF FAULTS

Type of fault	Specific phase	Boundary condition
Single line to ground fault 	A	$I_b = I_c = 0$ $V_a+I_aZ_d=0$
	B	$I_c = I_a = 0$ $V_b+I_bZ_d=0$
	C	$I_a = I_b = 0$ $V_c+I_cZ_d=0$
Double line to ground fault 	A	$V_b+I_b Z=V_c+I_c$ $Z = -(I_b+I_c)Z_d$ $I_a = 0$
	B	$V_c+I_c Z=V_a+I_a$ $Z = -(I_c+I_a)Z_d$ $I_b = 0$
	C	$V_a+I_a Z=V_b+I_b$ $Z = -(I_a+I_b)Z_d$ $I_c = 0$
Single phase open 	A	$I_a = 0$ $V_b+I_bZ = 0$ $V_c+I_cZ = 0$
	B	$I_b = 0$ $V_c+I_cZ = 0$ $V_a+I_aZ = 0$
	C	$I_c = 0$ $V_a+I_aZ = 0$ $V_b+I_bZ = 0$
Double Phase open 	A	$I_b = I_c = 0$ $V_a + I_aZ = 0$
	B	$I_c = I_a = 0$ $V_b + I_bZ = 0$
	C	$I_a = I_b = 0$ $V_c + I_cZ = 0$

III. BASIC NETWORK EQUATION

Basic equations for any n bus system may be given as [9]:

$$[Y_{bus}]V_{bus} = [I_{bus}] \quad (2)$$

where Y_{bus} is n×n admittance matrix and V_{bus} and I_{bus} are n×1 voltage and current vector respectively.
V_{bus} can be obtained by using equation (2)

$$V_{bus} = [Z_{bus}]\, I_{bus} \quad (3)$$

where $[Z_{bus}] = [Y_{bus}]^{-1}$ i.e. impedance matrix of size n×n.

In matrix form we can write the above equation as follows:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_1 & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (4)$$

where Z_1 and Z_2 are known as driving point impedance and Z_{12} and Z_{21} are known as transfer impedance [4].

Hence, when fault occurs anywhere on the system impedance matrix changes accordingly. This paper uses fault port matrix to calculate parameters related to simultaneous faults as given in [4]. According to the multiple port theory each fault point is considered as a port. In a port the current coming out of one terminal should be equal to the current entering another terminal [1].

IV. FAULT PORT MATRIX

In [2] although the short circuit fault was occurring but during simulating it the impedance matrix i.e. Z_{bus} was used unchanged. But usually we cannot consider it like that as the fault may occur at any point on the network. Always considering a fault point as an addition of bus may make the calculations difficult. Hence Z. X. Han has devised the method of fault port matrix which is easy to understand and lesser the computation time as well.

A. Fault port matrix elements

Taking case of a general short circuit fault at any point k on any line as shown in fig. 2 and assuming the injected

current to be I_k and voltage at that point be V_k the equations may be:

$$Vi - Vk = -rzij\ Ii \quad (5)$$
$$Vk - Vj = (1-r)zij\ Ij \quad (6)$$
$$Ii - Ij = Ik \quad (7)$$ where r is the distance between point i and k.

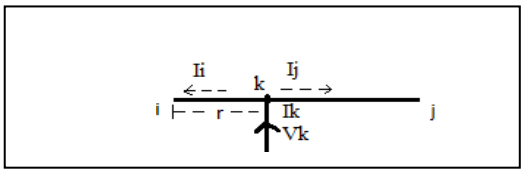


Fig. 1. Short Circuit fault at point k

In the formation of fault port matrix it is assumed that the unity current is injected at any bus m and the voltage at port k is equal to the impedance between m and k. Therefore,

$$V_k = z_{mk} = (1-r)z_{mi} + rz_{mj} \quad (8)$$ where Z_{mk} is the transfer impedance.

For finding the driving point impedance the equation is:

$$V_k = z_{kk} = (1-r)2\ z_{ii} + r2\ z_{jj} + 2r(1-r)z_{ij} + r(1-r)z_{ij} \quad (9)$$

If two short circuit faults are occurring simultaneously on the same line as shown in fig 3 then the transfer impedance can be given as:

$$z_{kkF} = (1-r)(1-r')z_{ii} + (1- \quad + \quad r(1- \quad r)r'z_{ij}$$
$$r')z_{ij} + rr'^{zjj} + r(1-r')z_{ij} \quad (10)$$

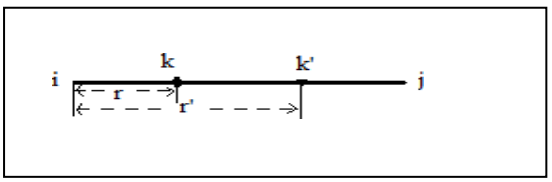


Fig. 2. Two short circuit faults occurring simultaneously at k and k'

If a short circuit fault and an open circuit fault occur simultaneously on the same line as shown in fig 4 then the driving impedance will be given as follows:

$$z_{kk} = z_{jj} + (1-r)\ z_{ij} \quad (11)$$

transfer impedance for the same will be given as:

$$z_{I\,II} = z_{ij} - z_{jj} - (1-r)z_{ij} \quad (12)$$

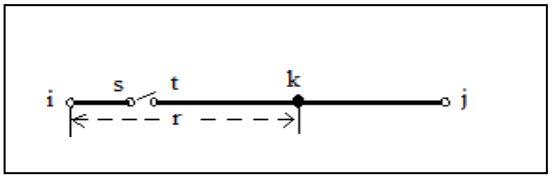


Fig. 3. Short circuit fault and open circuit fault occurring simultaneously

Further these equations are manipulated using the method given in [9]. Considering the line i-j is switched open and two sample buses s and t have been inserted in the circuit.

Method used in [9] demonstrates the modification of Zbus by addition and deletion of the bus. So here opening of line s-t will act as opening of the branch.

Transfer impedance between the fault point k and any bus m after opening of the branch is given as:

$$Z'_{km} = Z_{km} - (C_k - 1 + r)P^{-1}C_m \quad (13)$$ driving point impedance is given as:

$$Z'_{kk} = Z_{kk} - (C_k - 1 + r)^2P^{-1} \quad (14)$$ transfer impedance between fault point k and terminal t is given as:

$$Z'_{kt} = Z_{kt} - (C_k - 1 + r)P^{-1}(C_i - 1) \quad (15)$$ where the terms C_m, C_i, C_k and P can be described as:

$$C_x = Y^T_{i-j}\ Z'_{\alpha,x} \quad x=m,k,i \quad (16)$$

$$P = Y^T_{i-j}Z'_{\alpha\alpha}Y_{ij} - Y_{ij} \quad (17)$$

To understand these equations in a better way one may refer to reference [9].

B. Methods

The method given in this paper is the review of the method given by Z. X. Han in [4]. Considering N number of faults occurring out of which M are series faults and N-M are the parallel faults.

The equation for these faults may be given as follows [4]:

$$\begin{bmatrix} V_{S(i)} \\ V_{P(i)} \end{bmatrix} = \begin{bmatrix} Z_{SS(i)} & Z_{SP(i)} \\ Z_{PS(i)} & Z_{PP(i)} \end{bmatrix} \begin{bmatrix} I_{S(i)} \\ I_{P(i)} \end{bmatrix} + \begin{bmatrix} V_S^{(0)} \\ V_P \end{bmatrix} \quad (18)$$

where $V_{S(i)}$, $I_{S(i)}$ and $V_S^{(0)}$ are voltage, current and open circuit voltage of series type fault having size M×1.
$V_{P(i)}$, $I_{P(i)}$ and $V_P^{(0)}$ are voltage, current and open circuit voltage of parallel type fault having size (N-M)×1.
$Z_{SS(i)}$, $Z_{SP(i)}$, $Z_{PS(i)}$ and $Z_{PP(i)}$ are the impedance matrices of sizes M×M, M×(N-M), (N-M)×M and (N-M)×(N-M) respectively and i = 0,1,2 representing zero, positive and negative sequence network respectively.

Performing partial inversion on equation (18) we obtain the following equations:

$$\begin{bmatrix} V_{S(i)} \\ I_{P(i)} \end{bmatrix} = \begin{bmatrix} A_{SS(i)} & A_{SP(i)} \\ A_{PS(i)} & A_{PP(i)} \end{bmatrix} \begin{bmatrix} I_{S(i)} \\ V_{P(i)} \end{bmatrix} + \begin{bmatrix} V_S^{(0,0)} \\ I_P^{(0)} \end{bmatrix} \quad (19)$$

where $A_{SS(i)} = Z_{SS(i)} - Z_{SP(i)}Z_{PP(i)}Z_{PS(i)}$

$A_{SP(i)} = Z_{SP(i)} - Z_{PP(i)}^{-1}$

$A_{PS(i)} = Z_{PP(i)}^{-1} - Z_{PS(i)}$

$A_{PP(i)} = Z_{PP(i)}^{-1}$

$$V_S^{(0,0)} = V_S^{(0)} - Z_{SP(1)}Z_{PP(1)}^{-1}V_P^{(0)}$$

$$I_P^{(0)} = - Z_{PP(1)}^{-1}V_P^{(0)}$$

Since here simultaneous faults are considered therefore phase shifting transformers might be needed. Using equation (19)

$$\begin{bmatrix} V_{S(i)}' \\ I_{P(i)}' \end{bmatrix} = \begin{bmatrix} N_{S(i)} & 0 \\ 0 & N_{P(i)} \end{bmatrix} \begin{bmatrix} A_{SS(i)} & A_{SP(i)} \\ A_{PS(i)} & A_{PP(i)} \end{bmatrix} \begin{bmatrix} N_{S(i)} & 0 \\ 0 & N_{P(i)} \end{bmatrix}^{-1} \begin{bmatrix} I_{S(i)}' \\ V_{P(i)}' \end{bmatrix} + \begin{bmatrix} N_{S(1)} V_S^{(0,0)} \\ N_{P(1)} \; I_P^{(0)} \end{bmatrix} \quad (20)$$

where $N_{S(i)}$ and $N_{P(i)}$ are turn ratio matrices of the ideal phase shifting transformer having sizes M×1 and (N-M)×1 respectively.

According to the boundary conditions given in table 2 for series and parallel faults equation (20) can be further simplified as:

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} A_{SS} & A_{SP} \\ A_{PS} & A_{PP} \end{bmatrix} \begin{bmatrix} I_{S(i)}' \\ V_{P(i)}' \end{bmatrix} + \begin{bmatrix} N_{S(1)} V_S^{(0,0)} \\ N_{P(1)} \; I_P^{(0)} \end{bmatrix} \quad (21)$$

where

$$A_{SS} = \sum_{i=0,1,2} N_{S(i)} A_{SS(i)} N_{S(i)}^{-1}$$

$$A_{SP} = \sum_{i=0,1,2} N_{S(i)} A_{SP(i)} N_{P(i)}^{-1}$$

$$A_{PS} = \sum_{i=0,1,2} N_{P(i)} A_{PS(i)} N_{S(i)}^{-1}$$

$$A_{PP} = \sum_{i=0,1,2} N_{P(i)} A_{PP(i)} N_{P(i)}^{-1}$$

Solving equation (21) series fault port currents and parallel fault port voltages can be calculated as given below:

$$\begin{bmatrix} I_{S(i)} \\ V_{P(i)} \end{bmatrix} = - \begin{bmatrix} N_{S(i)} & 0 \\ 0 & N_{P(i)} \end{bmatrix}^{-1} \begin{bmatrix} A_{SS} & A_{SP} \\ A_{PS} & A_{PP} \end{bmatrix}^{-1} \begin{bmatrix} N_{S(1)} V_S^{(0,0)} \\ N_{P(1)} \; I_P^{(0)} \end{bmatrix} \quad (22)$$

Substituting equation (22) in equation (19) series fault port voltages and parallel fault port currents can be calculated.

This method has been computationally implemented and the results are shown in this paper using the algorithm.

V. FLOWCHART[4]

Below given is an algorithm implementing the above given method. First and foremost load flow is to be done to get the reference values to see the changes occurred after faults. Also, the open circuit voltage mentioned in equation (18) will be equal to the voltages obtained from the load flow. Hence, it is one of the major parts of the flowchart.

The admittance matrices formed here are sparse in nature. The computation time is saved using admittance matrix in load flow analysis. Then these matrices are transformed into impedance matrices for further calculation as the fault analysis generally uses z bus values for its calculations..

Once the type of the fault is specified we can proceed with the formation of fault port matrix. Fault port matrix is formed based on the method given above. Bus voltages and currents of the buses affected by occurrence of the fault are calculated. The value of currents and voltages are aligned with the boundary values.

Once a particular fault analysis is completed we can proceed with the other faults, if present. Else the algorithm stops and result is obtained.

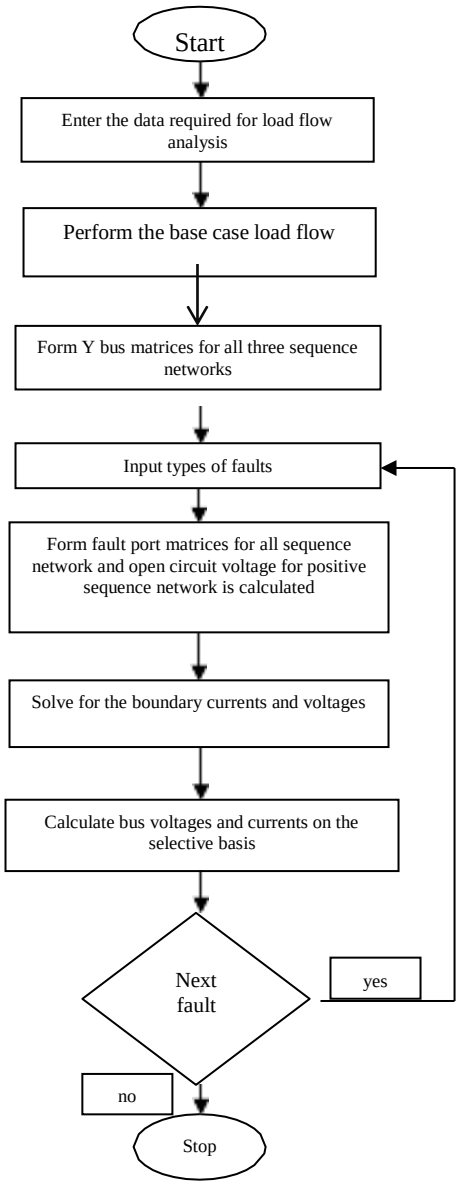


Fig. 4. Flowchart

VI. RESULT

Data for a four bus system was taken from [10] and the above method was implemented on that system. Giving different kinds of faults as input results are given below.

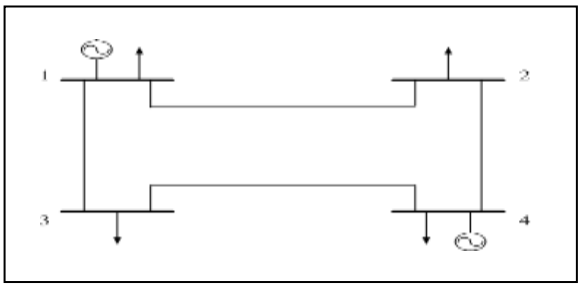


Fig. 5. Circuit Diagram

Fig. 5 shown above represents a four bus system whose line data and bus data are given below in table III and table IV.

TABLE III. LINE DATA

from bus	to bus	R	X	Y/2	R0	Xo
1	2	0.0101	0.05	0.05	0.003	0.013
1	3	0.0074	0.037	0.04	0.002	0.009
2	4	0.0074	0.037	0.04	0.002	0.009
3	4	0.0127	0.064	0.06	0.003	0.016

TABLE IV. BUS DATA

Bus	Pg	Qg	Pload	Qload	V(p.u)	Angle	type
1	0	0	50	30.99	1	0	1
2	0	0	170	105.4	1	0	2
3	0	0	200	123.9	1	0	2
4	318	0	80	49.58	1.02	0	3

For single line to ground fault occurring on bus 2 and 4 simultaneously as shown in fig. 6 fault port currents are given in table V:

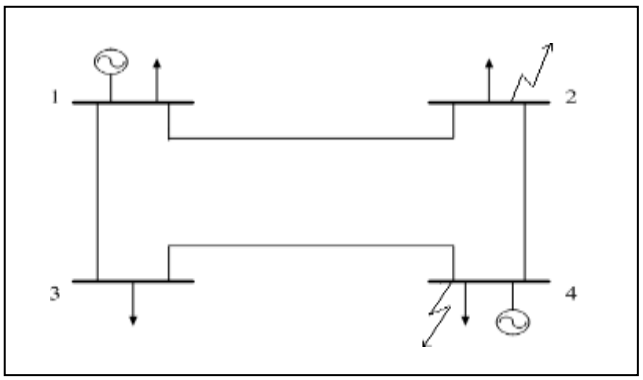


Fig. 6. Single line to ground fault on bus 2 and 4 simultaneously

Table V. THREE COMPONENTS OF FAULT CURRENTS

Bus No.	Positive Sequence	Negative Sequence	Zero Sequence
2	1.1672	1.1672	0.32661
4	1.1212	1.1212	0.2324

Fault port currents for a single line to ground fault on bus 2 and open circuit fault on bus 4 is shown in fig. 7:

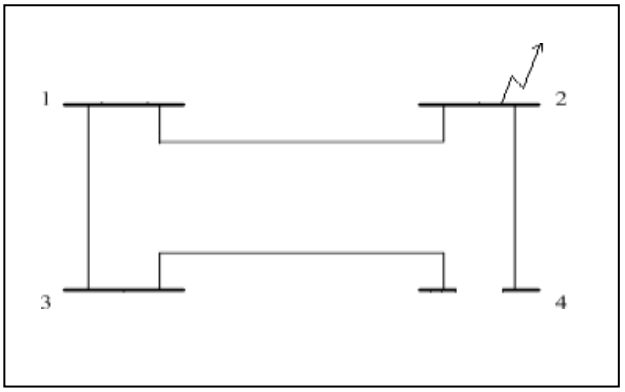


Fig. 7. Single line to ground fault on bus 2 and open circuit fault on bus 4

The fault port currents for the above mentioned condition is given in table VI.

TABLE VI. THREE COMPONENTS OF FAULT CURRENTS

Bus No.	Positive Sequence	Negative Sequence	Zero Sequence
2	0.064093	0.064093	0.064247
4	0.031969	0.031969	0.031969

VII. CONCLUSION

The generalized method for doing simultaneous fault analysis have been discussed and results of calculated fault port current and voltages have been shown.

REFERENCES

[1] P. M. Anderson, Analysis of Faulted Power Systems, The Iowa State University Press, 1973.

[2] G.GROSS, H.W.HONG, “A two-step compensation method for solving short circuit problems”, IEEE Transaction on Power Apparatus and Systems, vol.PAS-101, pp. 1322-1331, 1982.

[3] G.GROSS, H.W.HONG, “A two-step compensation method for solving short circuit problems”, IEEE Transaction on Power Apparatus and Systems, vol.PAS-101, pp. 1322-1331, 1982.

[4] Z.X. Han, "Generalized Method of Analysis of Simultaneous Faults in Electric Power System". IEEE Transactions on Power Apparatus and System &, Vol PAS-101, pp. 3933-3942, October 1982.

[5] V.BRANDWAJN, W.F.TINNEY, “Generalized method of fault analysis”, IEEE Transaction on Power Apparatus and Systems, vol.PAS-104, pp. 1301-1306, 1985

[6] R.BUALOTI, P.Pugliese, F.Torelli, M.Trovato,”A Generalised Method For Simultaneous Fault Analysis”, MELCON-96,8th Mediterranean Electrotechnical Conference, pp 721-725, 1996

[7] J. R. Mortlock,"The Evaluation of Simultaneous Faults on Three Phase Systems", Journal of Institution of Electrical Engineers-Part II : Power Engineering,, vol. 94, pp. 166-190, 1947

[8] T. E. DyLiacco and K. A. Ramarap, "Short-circuit calculation for Multiline Switching and End Fault", IEEE Transaction on Power Apparatus and systems,vol. PAS-89, No.6, pp.1226-1237, 1970.

[9] M.Etezadi-Amoli, "Simultaneous Fault Analysis Using The Generalised Method of Fault Analysis", Proceedings of the Twenty-First Annual Norht American Power Symposium, pp 188-191, 1989

[10] John J. Grainger and William D. Stevenson, Jr, Power System Analysis,McGraw-Hill Publication, Inc.