IMPLEMENTATION OF EFFICIENT CODE CONVERTORS USING REVERSIBLE LOGIC GATES

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ABSTRACT:

In today's digital era, power saving is a thrust area of a handheld device that is operated in a battery-powered source. Low power design has been achieved in various types of design strategies by the VLSI designer. One among those the reversible logic designs has been one of the promising technologies gaining greater interest in the design because of less dissipation of heat and low power consumption. In digital circuit design, code converters play a significant role in data transfer and data processing. These converts use fewer hardware resources, minimal switching activities, enhanced processing capabilities etc. In this paper, we proposed the simplified code converter, namely Binary to gray, gray to binary, binary to excess 3 and Excess 3 to binary model, using the basic reversible logic gate with minimal no of gates and minimal critical path.

Keywords: Reversible logic, code converters, low power design

1. INTRODUCTION

Reversible logic has presented itself as a prominent technology that plays an imperative role in Quantum Computing. Quantum computing devices theoretically operate at ultrahigh-speed and consume infinitesimally less power. The reversible computing mostly used in the low power design technology which is the prominent technology in the filed of quantum computing, Nano technology, Optical computing.

Research has done in this project aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realise Quantum computing devices. To authenticate this research, various combinational and sequential circuits are implemented such as a 4-bit Ripple-carry Adder, (8- bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of an 8-bit GCD processor using Reversible gates. The power and speed parameters for the circuits have been indicated and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are faster and power efficient. The designs presented in this project were simulated using Xilinx 14.1 software.

2. LITERATURE SURVEY

Landauer, Rolf,(2000) states that computing machines inevitably involve devices which perform logical functions that do not have a single-valued inverse. The logical irreversibility is always associated with the physical reversibility. These irreversibility requires the minimal heat generation while computing the data or the information during the machine cycle. This heat generation in the order of the $\mathbf{K_b\,T}$ ln2. In 1973 Benet CH explained that the logic reversibility in general computation which leads to new era of the logic reversibility. In irreversibility lacks of single valued inverse operation. The logic reversibility retain their simplicity operation. B,Raghu Kanth; B,Muarali Krishna;G,Phani Kumar;J,Poornima has studied the comparative study of Reversible logic gates in the low power design. :the about the Reversible Logic in 2012,.

Nachittigal, M.;Thapliyal, H.;Ranganathan, N., in 2010 discussed about floating point multiplication which is one of the major operations in image and digital signal processing applications. The single precision floating-point multiplier requires the design of efficient 24x24 bit integer multiplier. In this work.

3. BASIC REVERSIBLE LOGIC

A.TERMINALOGY

Some of the basic terms used in reversible logic is described below :

- **Reversible Logic Gate :** A reversible logic gate is an one to one mapping between the input to output. For, example N-input N-output logic device that provides one to one mapping between input and output of N values. It not only helps us to determine outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.
- **Garbage outputs(GO) :** It is the additional outputs which can be added to output side. It makes that the number of input and outputs equal whenever necessary. The outputs which are not used in the synthesis of a given function are called Garbage outputs.
- **Quantum Cost :** This refers to the cost of the circuit in terms of the cost of a primitive gate. It is computed knowing the number of primitive reversible logic gates(1*1 or 2*2) required to realize the circuit. It gives the total computation cost of the circuit
- **Constant inputs(CI) :** It is also called as the ancilla which is used to maintain the one to one mapping. It has either one or zero value.

B.Basic Reversible logic gates

The basic reversible logic gates that are widely studied in the reversible logic are shown below.

Feynman Gate : Feynman gate is a universal gate which is used for signal copying purposes or to obtain the complement of the signal.

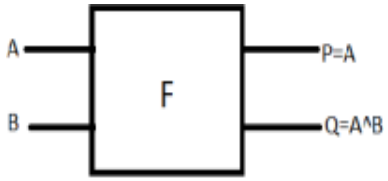


Fig1 : Feynmann gate

Peres gate : It is a basic reversible gate which has 3-inputs and 3-outputs.

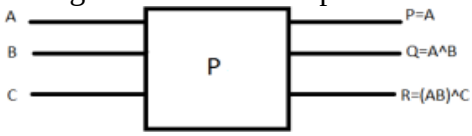


Fig 2 : Peres gate

HNG Gate : HNG gate is a reversible gate which has four inputs mapped to four outputs.

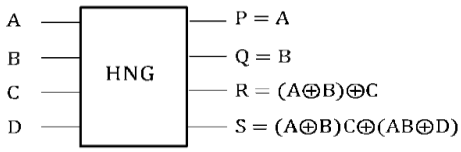


Fig 3 : HNG gate

4. EXISTING SYSTEM :

In modern computers, computation is performed by assembling together set of logic gates like AND, OR, XOR, processing two logic inputs and yielding one logic output, are often addressed as irreversible logic gates. For example, if we considered the full adder having three inputs A,B,C producing two outputs as sum and carry in irreversible gates.

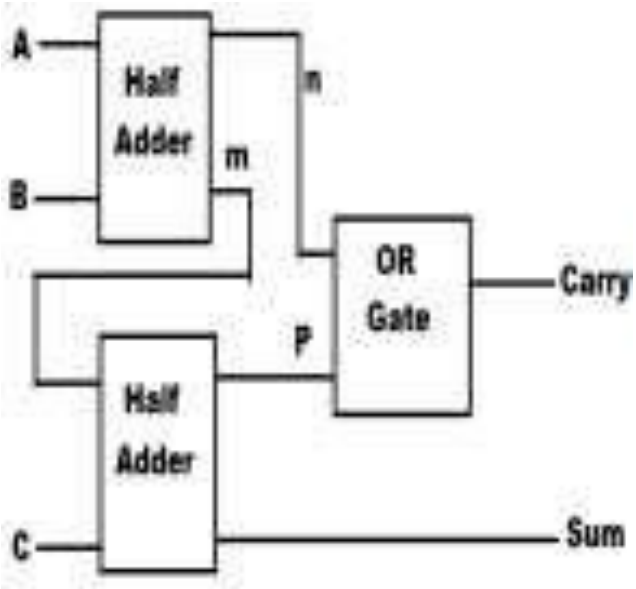


Fig 5 : Irreversible Full Adder

In reversible gates the number of inputs are equal to number of outputs. Simlarily if we consider the full adder in reversible gates for A,B,Cin,0 as input we get the sum and carry as output along with garbage output G1,G2.

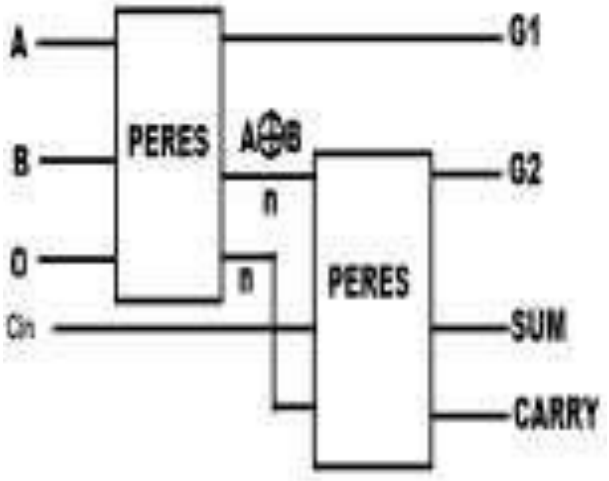


Fig 6: Reversible Full Adder

5. PROPOSED SYSTEM

Designing of reversible logic circuit is challenging task, since not enough number of gates are available for design. Reversible processor design needs its building blocks should be reversible code converters became essential one. A code is basically the pattern of these 0's and 1's used to represent the data. Code converters are a class of combinational logic circuits that are used to convert one type of code in to another. Some of the most prominently used codes in digital systems are Natural Binary Sequence, Binary codes Decimal, Excess-3 code, Gray code, ASCII code etc. Like any combinational digital circuit, a code converter can be implemented by using a circuitary of AND, Or and NOT gates. Here in this paper focuses more on conversion of code between binary to gray and binary to excess-3.

a. Reversible Binary To Gray And Gray To Binary Code Converter

Binary to Gray code converters used to reduce switching activity by achieving single bit transition between logical sequences.

The circuit is constructed with the help of Feynman gate(FG) and the figure shows the circuit diagram of reversible Binary to Gray and Gray to Binary code converter.

Fig : Circuit diagram for Reversible Binary to Gray code converter

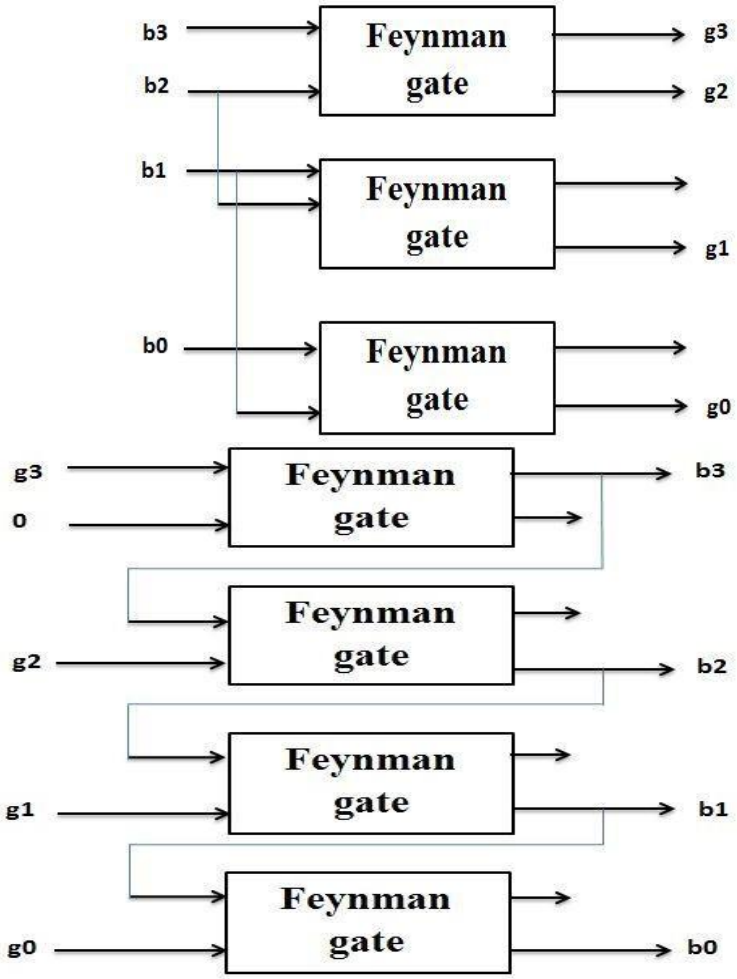
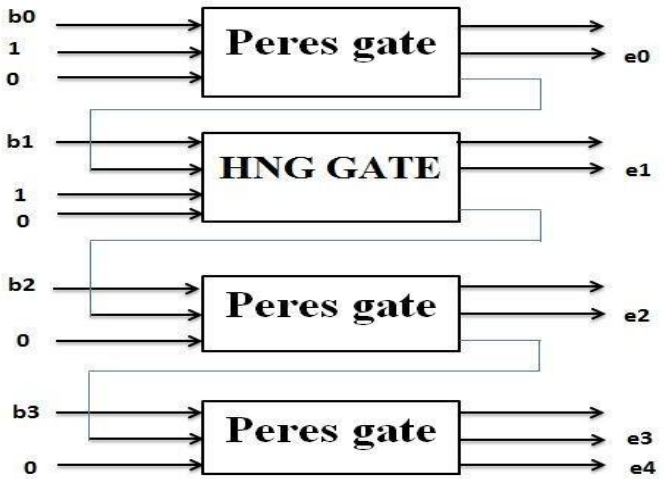


Fig 7 : Circuit diagram for Reversible Gray to Binary

b. Reversible Binary to Excess-3 and Excess-3 to Binary code converter

Binary to Excess-3 code converter used in arithmetic operational circuits to reduce the overall hardware complexity, The circuit is constructed with the help of three reversible gates Feynman gate and HNG gate and the figure shows the circuit diagram for Bianry to Excess-3 and Excess-3 to Binary code converter.

Fig 8 : Circuit diagram for Reversible Binary to excess-3 converter



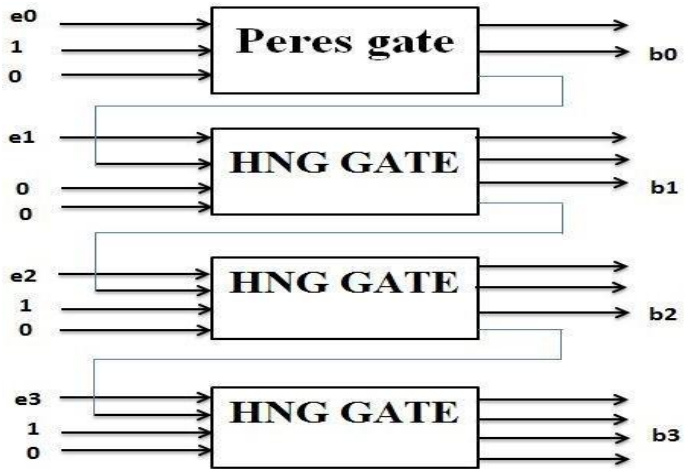


Fig 9 : Circuit diagram for Reversible Excess-3 to Binary converter

6. SIMULATION RESULT AND ANALYSIS

The simulation is done on ISE-Simulator with 14.1. The circuit converters the Binary number to its equivalent Gray code. Similarly Gray to Binary conversion is simulated.

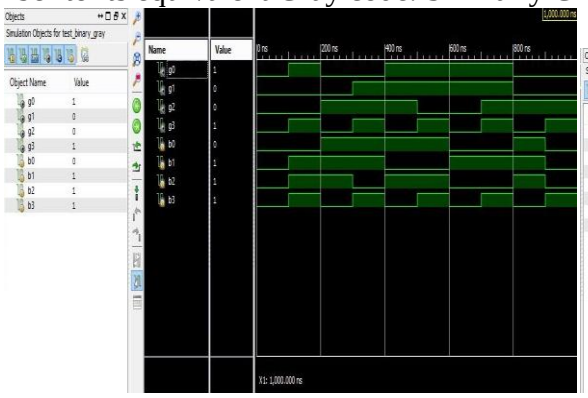


Fig 10 : Simulation result of 4-bit Binary to Gray code


Fig 11 : Simulation result for 4- bit Gray to Binary code

Similarly the Simulation is done on the circuit converters the Binary to Excess-3 and Excess-3 to Binary code converter

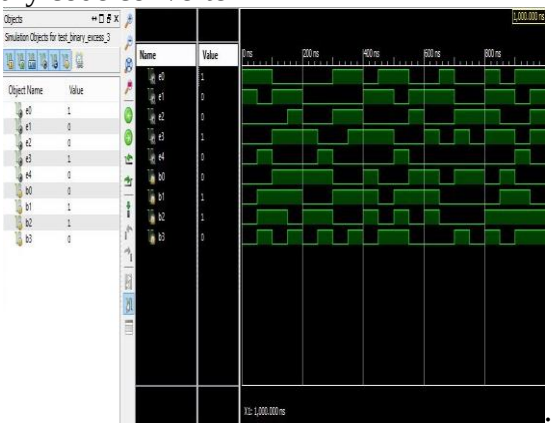


Fig 12 : Simulation result for 4-bit Binary to Excess-3 converter


Fig 13: Simulation result for 4-bit Excess-3 to Binary code

7. CONCLUSION

This paper has introduced and proposed reversible logic gates and reversible circuits for realizing different code converters like Binary to Excess-3,Excess-3 to Binary, Binary to Gray, Gray to Binary using reversible logic gates. The proposed design leads to the reduction of power consumption compared with conventional logic circuits, the design proposed is implemented with

FG and URG gates only in near future with the invent of new RLG the power consumption may reduce to little more greater extent, not only that there will be a chance of implementing different logic circuits using reversible logic gates and which intern helps to increase the energy efficiency to a greater extent.

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