A REVIEW ON LOW POWER AREA-EFFICIENT ARCHITECTURE FOR LINEAR FEEDBACK SHIFT REGISTERS

Lingala Srinivas, Lecturer in ECE, Dr BR Ambedkar GMR polytechnic for women karimnagar
Chandrakala, M.Tech
G kiran kumar Lecturer in physics Dr BR Ambedkar GMR polytechnic for women karimnagar

Abstract: ***This paper describes low power design and implementation of Linear Feedback Shift Register (LFSR). The easiness in implementation and simple operation of Linear Feedback Shift Register have made it fit into a wide range of digital systems design. Since random pattern generation, data encryption and decryption play a major role in communication systems, the LFSR comes into view for developing the patterns forthese applications. As the need increases day after day, simple andhigh-performance design of LFSR is required. As power consumption of the device being an important factor in the VLSI circuits, it has to be reduced by including power optimization techniques in the designs. Pulsed Latch is a popular technique of reducing power consumption which uses Pulsed Latches instead of flip-flops. As latches have lesser number of circuit elements compared to flip-flops, the area is also minimized. By implementing this pulsed latch technique, the linear feedback shift register can be designed with low power and area. The design entry is done in VHDL code and implemented using Cadence tool. In Cadence, Nclaunch, RTL Complier and Encounter tools are used for simulation, synthesis and implementation. With this method, the power reduction is achieved up to 41.99%***

Index Terms: Linear Feedback Shift Register, Patterngeneration, Pulsed latches, low power VLSI.

I. . INTRODUCTION

The highly emerging digital VLSI system design in the communication field requires fast generation of random patterns for error detection, VLSI circuits testing, data encryption and decryption. The test patterns for the above applications are generated by Linear Feedback Shift Register(LFSR). The 8 bit pattern generation circuit to generate a pattern X^7+X^5 +X^4+X^3+1 is shown in Figure 1. As the technology advances, the need for low power consumption circuit increases. Thus, the circuit is generally expected to be designed in such a way that it should consume less power, occupy minimum area with improved response time. The useof flip-flop with activated clock in the register design consumes more power which is not sufficient for high throughput, so pulsed latches are used in the place of flip-flops in this proposed work.

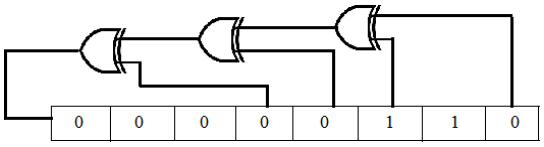


Figure 1. 8-bit LFSR circuit

For reducing the power consumption of the device, various methodologies are available in the literature. Dropping the number of transitions is one of the means for power optimization. Transitions are reduced by swapping the bits and applying clock to half part of the circuit. Clock gating is also employed for power optimization. Although various optimization techniques are implemented for minimizing thepower consumption of the device, they are not eventually much effective by the means of reducing the response time and area. Like

power optimization techniques, techniques forminimizing the area and increasing the speed are also employed in [1]-[5]. The conventional method of serial to parallel architecture and pipelining algorithms are used to increase the speed of the shift register. Also calculation of output value only by considering the past feedback value in the transposed serial architecture, increases the speed. The transformation from long LFSR sequence to several short LFSR sequence in series reduces the overhead. Though several techniques are used to reduce the power, area and speed, they are not efficient in terms of critical path delay. Hence, a new architecture for LFSR using pulsed latches is proposed for pattern generation in which all the three parameters mentioned above are optimized. The paper is structured as follows. The methodologies adopted for power, area and speed optimization are reviewed in section II, proposed methodology is explained in section III and the results are analyzed in the section IV. The paper is concludedin chapter V.

II. PREVIOUS METHODOLOGIES

A. Power Optimization Techniques:

Linear feedback shift register is the main component used inself-tests of integrated circuits. D flip-flop is playing a majortask in the LFSRs. To shrink the power consumption of the Dflip-flop, different architectures are followed in CMOS technology. Three types of LFSR architectures are implemented with NAND gates, pass transistor and transmission gates [6] .Among

that the pass transistor has smallest power consumption, smallest number of transistor and layout area. Clock gating is one of the methods to minimize the power consumption in the linear feedback shift registers. The authors in [7] proposed a method to provide a significant power reduction based on the clock design approach that depends on the technological characteristics of the used gates. In modified LFSR with clock gating, the power consumption was reduced by disabling the clock signal applied to the flip-flop when the output signal is equivalent to the input signal. By using this method, 20% of maximum power and 30% of average power reduction is achieved. In a modified clock scheme proposed in [8][9], two n/2-bit LFSRs are used in building n-bit LFSR. Mostly, a clock with half of its normal speed is used in activation of one portion of the D flip-flops in the TPG during one clock cycle. The second parts of the D flip-flops are activated by another clock with same half speed during the next clock cycle. These two clock signals must be synchronized with a master clock signal and have shifted-in time period of same value. At every clock cycle of the test phase, only half of the circuit inputs could be activated when a test vector is applied to the circuit under test (CUT). As a result, the peak power as well as the average power used in the CUT is minimized. Besides, the power consumption in the Test Pattern Generation (TPG) is also reduced. In [10], LFSR is designed for proving reduced power dissipation when testing is performed. The association between the successive patterns is superior for the period of normal mode than test mode. This approach incorporated the idea of minimizing the number of transitions in generated test patterns. The transitions are minimized by increasing association between consecutive bits. It is observed that the output dynamic power is reduced by 44.6 %. The cumulative power consumption in modified LFSR is 46% which is lower than that of normal LFSR. In [11], the author reviewed that during the test phase in BIST, the power dissipation is greater than the functional power, which has an effect on the reliability of the integrated circuits. This is because the test patterns generated by the patterns generator have low correlation. So, a stepped segment LFSR is proposed which is a low transition TPG allowing utmost two transitions between the successive test patterns. This LFSR reduces the testing power by 19.63% on average with slight drop in fault coverage. In [12], the design of LFSR is done in sub threshold regime which requires Delay flip flops and XOR gates during its realization. With various D flip-flop and XOR gate realizations, four different LFSR structures were created. One of the architectures uses true-single phase clock D flip-flop and static CMOS XOR gate. Transmission Gate based XOR gate and TSPC D flip-flop are used in the second design. The two other architectures use transmission gate based D flip flop with static CMOS XOR gate or transmission gate based XOR gate. Comparing the performance of these architectures with respect to highest frequency and power consumption, it is found that, the LFSR employing TSPC based D flip-flop are capable of operating at highest operating frequency with low power. The power consumption achieved is in nano watts. In [17], low power test pattern generator, designed using the interpolation of the interceder pattern is proposed with a transition controller module. It uses using Low Transition Generalized Linear Feedback Shift Registers.

This increases the interrelation between successive patterns. In this method, the number of transitions is reduced by swapping the bits and also by bypassing some of the flip-flops in the scan chain. By doing this, significant power reduction in the dynamic power is achieved. This method reduces the switching between sequent test pattern thereby reducing power. Another low power test pattern generator is designed in [13] using LP-LFSR (low power linear feedback shift register). It has counter, gray code generator, Braun array multiplier and an EX-OR gate. As Pipelined Braun array multiplier is faster than non-pipelined multiplier, it is selected. As in all other cases, energy and power consumption largely rely on the switching behavior, clock frequency and power supply voltage. This method is proposed to reduce the count of switching activities at the input sides of the circuit that is under test. As the power dissipation during testing mode is high compared to normal mode of operation, low power LFSR using gate diffusion input (GDI) technique is designed in [14]. Various combinational synchronous functions could be implemented using this technique with no more than two transistors. Therefore, this technique is suitable for implementing low power, fast circuits with least number of transistors while leading to advancement in static power characteristics and logic level swings. Based on this approach, GDI technology reduces hardware by 20% and power dissipation by 45.4%.

B. Speed optimization Techniques:

The parallel architecture mainly leads to high throughput of any design. There are various techniques in which the design is employed in parallel architecture to increase the device speed. One such architecture is employed in [2]. In this work, the serial architecture of LFSR is transformed to parallel architecture. The parallel architectures presented previously computed values using past inputs and register outputs. But this parallel architecture, which is based on the transposed serial LFSR calculates the output using only the past feedback values. Consequently the area-time product decreases up to 59% compared to other architectures. Although the various optimization techniques are fairly effective in reducing the complexity of hardware architectures, it is not adequate for reducing the delay in critical paths. Architecture with partial pipelining was proposed to overcome this problem in which a state-space transformation is conducted to the conventional parallel LFSR. On the other hand, this approach increases the hardware complexity, since additional hardware components are needed for the transformation. Jaehwan et al proposed a parallel LFSR architecture derived from the transposed LFSR [2] to eliminate redundant calculations and registers, thereby reducing the critical path delay and the hardware cost. It reduces the number of XOR gates, registers leading to shortened critical path. In the references [3]-[5], the design of parallel LFSR architecture

based on parallel Infinite Impulse Response filter design is presented which operates at high speed. Its contribution is twofold. At first, transformation is done from serial architecture to parallel LFSR architecture. Then the parallel LFSR is modified into the form of adaptingto pipelining and retiming algorithm. With increase in cost ofhardware overhead, parallel transformation achieves a betterspeed improvement compared to serial architecture. The retiming and pipelining algorithms reduce the critical path in the parallel architecture and thus reducing the hardware cost. Even though parallel processing architectures increase the number of message bits, it leads to lengthy critical path. Longer the critical path, esser is the speed of operation and so the throughput achieved using the parallel processing architecture is reduced. Hardware expenditure is another problem in this parallel architecture. All these disadvantages can be overcome by a scheme based on look ahead computations, retiming and pipelining. Using the parallel and pipelined IIR filter design, critical path in the parallel architecture is reduced. The above techniques diminish the critical path delays without increasing in hardware cost. This design can be applied to any LFSR architecture.

III. PROPOSED ARCHITECTURE

In the proposed method, the flip-flops which are the combination of master and slave latches are replaced with thepulsed latches. The clock pulse which is a continuous periodicwaveform is replaced with a pulse generated by the pulse generator circuit shown in Figure 2 to activate the latch. Thepulse generator circuit is made up of two basic gates AND andNOT. The inputs to the AND gate are clock pulse and an inverted clock pulse for which NOT gate is used. The invertedclock pulse reaches the AND gate after sometime because while passing through the invertor it acquires some delay. The proposed LFSR is shown in Figure 3.In the feedback path ofLFSR, the Exclusive-OR (EXOR) gate is used which has twoinputs taken from appropriate bit positions.

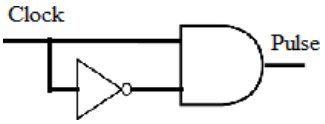


Figure 2. Pulse generator circuit

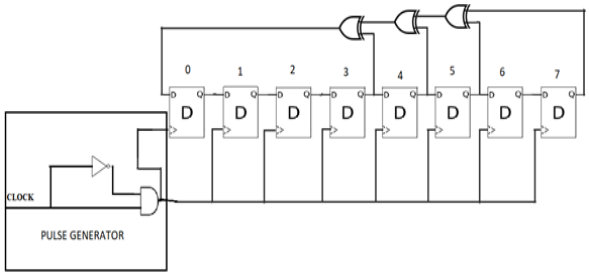


Figure 3. Proposed 8 bit LFSR circuit

Thus the eight D-latches, three EXOR gates and the pulse generator circuit are used in construction of the LFSR circuit. The initial value stored in LFSR is seed which is always set tobe a non-zero value. For n-bit LFSR 2n -1 patterns areobtained. In the above 8-bit LFSR circuit, the taps are taken from (7, 5, 4, 3) bit positions to generate polynomial and 255patterns are obtained. During the operation of above circuit, timing problem arises. This problem is due to the same pulseis given to all the latches. The output signal arrives at the firstlatch properly in time. But the outputs at the other latches areexact.

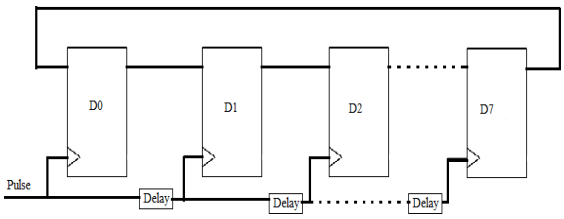


Figure 4.a Delayed pulse circuit

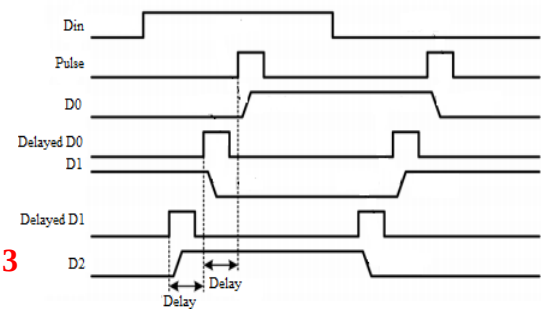


Figure 4.b Output of the LFSR with delayed pulse circuit

The solution to solve this problem is to generatenon-overlapping pulses and introduce them in the clock pathof each latch as in Figure 4.a. Another solution to this problem is to introduce a delay circuit between the latches where the output of first latch is delayed to the clock period and given to the second latch as in Figure 5a. The output fromthe first latch to second latch changes when the pulse is highas shown in Figure 4 b, 5.b. Thus by implementing any one ofthe solution the timing issues can be solved. In the proposed architecture, the delayed pulse method is used. To solve the timing problem, the taps are taken from the appropriate bit positions. In the conventional delayed pulse circuit shown inFigure 4a, the width of the pulse applied to all the invertors ofdelay circuit must be larger than the sum of rising and the falling time periods to keep the shape of the pulse. But in theproposed delay circuit the pulse width can be smaller than thesummation of the rising and falling time period as sharp pulses are produced from AND gate.

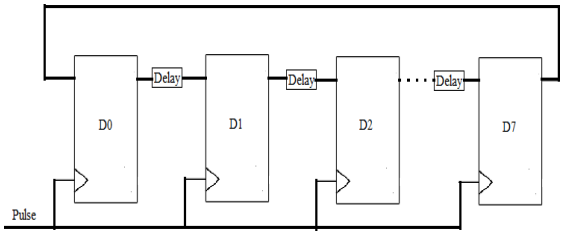


Figure 5.a LFSR with delayed output circuit

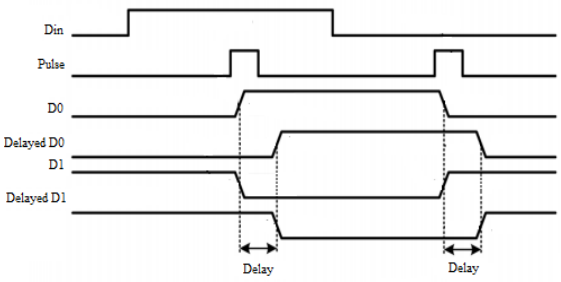


Figure 5.b Output of the LFSR with delayed circuit

Hence, this delayed pulse generator circuit is suitable for short pulsed clock signal circuits. Only the latches and the pulse generator circuits consume power. This reduces the power and the number of clock signal. This technique can be used in data compression and security applications proposed in[15] and signal processing applications proposed in [16]. This proposed architecture can also be applied during testing methodologies of VLSI circuits [17-20] and for different algorithms used in creating LFSR based architecture forrandom pattern generation[21].

IV. RESULTS AND ANALYSIS

A. Results

For the simulation process of LFSR, the Nclaunch tool is used. After the simulation process, the sim waveform appears as in Figure 6. By depositing the input values, the output is obtained.

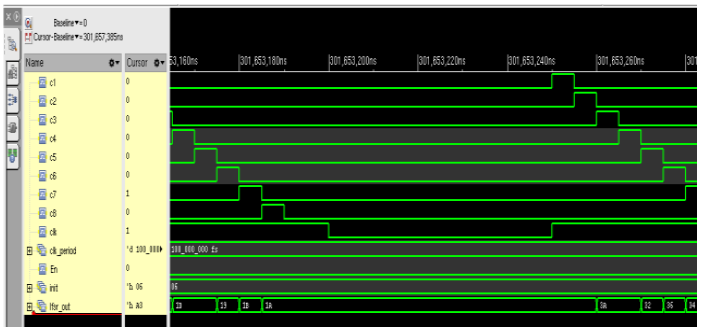


Figure 6 Simulation output

Figure 6 shows the simulation output obtained using nclaunch tool. From this design, pulses with different time patterns are obtained. For the given input value of 6, the different output patterns generated are 1D,19,1B,1A,8A,32,36,34. Using RTL compiler, netlist, constraints are generated and the obtained schematic of D latch and LFSR are shown in Figure 7 and Figure 8 respectively.

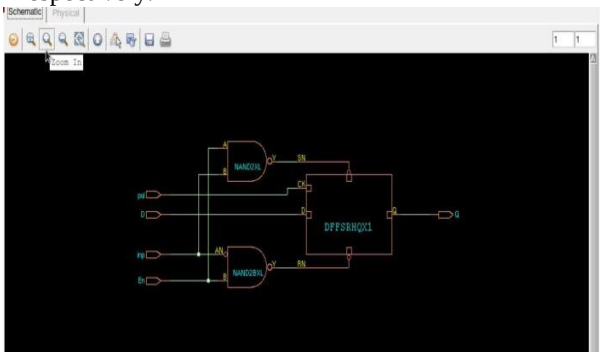


Figure 7 RTL schematic of D latch

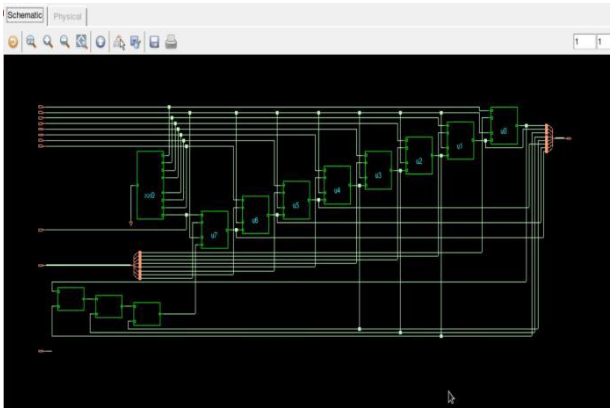


Figure 8 RTL schematic of proposed LFSR

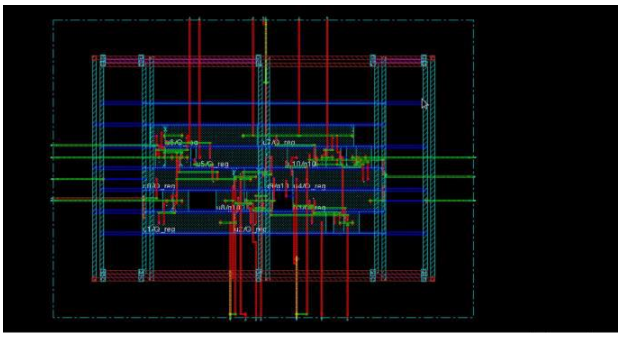
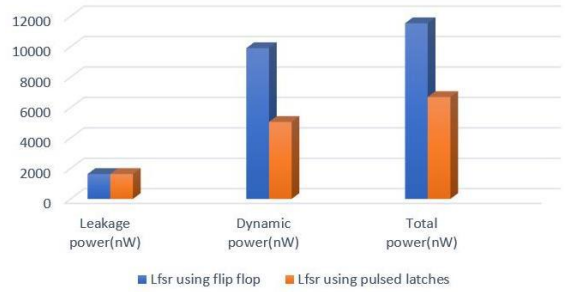


Figure 9 Layout of LFSR

The above Figure has eight latches from u0 to u7, three XOR gates and a pulse generator. After doing the physical design processes like floor-planning, placement and routing along with timing analysis, the layout is created and is shown in Figure 9. Finally GDSII is created.

B. ***Analysis of Design parameters***



In VLSI circuits, the power is the major factor which has been addressed in this paper. In the proposed method clock signal was replaced with the pulses to trigger the latches and also the D flip-flop with the D latch. Only the latches and the pulse generator consume power. This minimizes the dynamic power measurably. The leakage power remains the same when compared to the conventional LFSR. As shown in Figure 10, that shows the power comparison chart, the total power is reduced considerably. The operating speed of LFSR has got increased as latches are used. The delay produced in the proposed LFSR is 65ps and in the conventional LFSR is 1230ps. The area of the proposed architecture remains the same.

V. CONCLUSION

This work provides new low power architecture for Linear Feedback Shift Register. The proposed architecture replaces the D flip-flop which is activated by clock with pulsed D latches. The power consumption and delay of the circuit got reduced because of the use of pulsed latches. This pattern generation by LFSR can also be used in data encryption circuits to provide security for generation of binary sequence. It is also used in retrieving the data after recombination and reception. This proposed LFSR may be extended for Data security and direct sequence spread spectrum applications.

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