

LOW POWER ALU DESIGN AND IMPLEMENTATION USING CLOCK GATING AND CARRY SELECT ADDER

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ABSTRACT

CPUs in general-purpose personal computers, such as desktops and laptops, dissipate significantly more power in the order of few watts because of their higher complexity and speed. ALU is a fundamental building block of CPU. It does all process related to arithmetic and logic operations. As the operations become more complex, the ALU become more complex, more expensive, takes up more space in the CPU and contributes more power dissipation within the CPU. Hence power consumption of ALU is a major issue in the designing of CPU.

In this paper, it is proposed to design an ALU with latch free clock gating technique to reduce clock power and dynamic power by turning off unused areas while working on one area of design to achieve low power consumption and the results are compared with ALU without clock gating. And also further improvement in power is expected by using a carry select adder (CSLA) as the primary computational element of the arithmetic unit for fast arithmetic operations. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 16-bit square root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. In this paper a low power 16 bit ALU is designed with HDL programming and then implemented on Xilinx Spartan 3EFGPA.

Key words: Low Power, ALU, Dynamic Power, Clock Power, Clock Gating, Carry Select Adder (CSLA), FPGA, HDL Programming.

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1. INTRODUCTION

Day by day the advancement in technology leads to increase in the number of transistor count on any digital logic design. This increase in transistor count have an sever impact on power consumption because adding more and more transistor will give rise in the heat dissipated in the device [1]. Now a days the era is revolving around portability, is offered by low power consuming system, Since most of the portable devices are battery driven the power consumption of these devices must be low so the battery life improves, performance improve, reliability improves and reduces heat removable costs. Because of these reasons the optimization for lower power dissipation and faster device performance is of prime concern in any design. The ideal design is one which consumes minimum power, requires minimum area but has the highest throughput. However, these parameters (area, speed and power) are often in disagreement and a suitable solution for this is to maintain a tradeoff between these

parameters. At every level of digital design flow there is a possibility in optimization of power even though benefits are good at the algorithmic and architectural design level.

In Modern day microprocessors design, maximum speed and low power with minimum area are main design constraints to meet performance requirement with technology. An Arithmetic and logic unit (ALU) is a digital electronic circuit that performs arithmetic and bitwise logical operations on integer binary numbers. ALU is the heart and crucial building block of all computationally intensive units such as central processing unit (CPU), Floating point unit (FPU) and Graphical processing unit (GPU), almost always falls in the data path during the execution of an instruction decoded by instruction decoder. To meet these requirements, a power efficient, high performance ALU need to be designed. Hence the power consumption of the ALU should be kept at a minimum.

2. SOURCES OF POWER DISSIPATION

There are several factors contributing to the CPU power consumption; they include dynamic power consumption, short-circuit power consumption, and power loss due to transistor leakage currents.

$$P_{CPU} = P_{dyn} + P_{sc} + P_{leak}$$

These powers are mainly classified as below two powers such as:

2.1. Dynamic power dissipation

Dynamic power dissipation of CMOS circuit has two parts - dynamic switching power and short circuit current power [2].

Dynamic switching power is dissipated every time the logic state of the gate changes. It is represented as $P = n f C V_{dd}^2$, where f is the frequency of switching, C_L is the load capacitance, V_{dd} is supply voltage and n is the probability of switching.

This power can be reduced by lowering switching frequency; however it is not desirable as it limits the speed of operation of the device. n can be reduced by reducing redundant switching activity. V_{dd} can also be reduced, however it leads to increased propagation delays and hence not desirable. Hence a proper tradeoff must be met between these parameters to obtain satisfactory device performance.

Short circuit current power is dissipated when both the NMOS and CMOS MOSFETs are partially on, during a switching activity. In this case a direct short circuit path is momentarily formed between power supply and ground, leading to significant power dissipation. This can be controlled by regulating the slew rate and applying sharp clock edges. However, generating such a clock is difficult.

2.2. Static or quiescent power dissipation

Static or quiescent power dissipation is independent of the switching activity of the circuit. This is caused due to leakage current in the device during steady state. Sub-threshold conduction is the reason for this power dissipation and can be controlled by biasing the MOSFETs well below their threshold voltages and using multiple threshold CMOS designs.

In this paper a 16 bit ALU is designed in VERILOG and clock gating (CG) technique is used to achieve lower power consumption is discussed in section III. And Also carry select adder with variable block length is used as the primary computational element of the arithmetic unit for further power reduction is discussed in section IV. The design is then simulated in ISim simulator and finally implemented in Xilinx Spartan 3E FPGA. The results are compared with that of a conventional ALU without clock gating, which revealed significant improved performance of the clock gated ALU over the conventional design is discussed in

section. The results are shown in section VI. The Concluding remarks and future scope of the technique is discussed in section VII and VIII.

3. CLOCKGATING

Power can be reduced in several ways such techniques include voltage reduction, frequency reduction, capacitance reduction, clock gating, using adiabatic logic and energy recovery logic. The motivation of using the clock gating (CG) technique is: as the ALU is the unit that performs arithmetic and logical operations, and no both the operations are performed at the same time. Hence, the clock can be provided to that unit which needs to be functional. This concept leads to the application of clock gating technique to the ALU. Another reason, Clock power is a major component of dynamic power dissipation [3]. In a synchronous circuit several modules are clocked at the same time. However, at any particular instant only single module may be functional. Hence the unnecessary clocking of the other modules lead to a lot of power dissipation. In a clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation by adding extra hardware to the circuit. Hence the unnecessary charging and discharging of the unused circuit that do not perform any active computation is avoided. Thus the clock gating technique is used to reduce the dynamic power.

- There are many clock gating styles available to optimize power in VLSI circuits. They can be:
- Latch-free based CGdesign.
- Latch-based CGdesign.

3.1. Latch-free Clock Gated ALU design

Clock gating is achieved by ANDing the clock signal with a control signal to form a gated clock, which is then applied to different components of the circuit. To which module the gated clock should be applied is decided based on the control signal.

Clock Gate = Clock signal [Gate (either AND or OR)] control signal

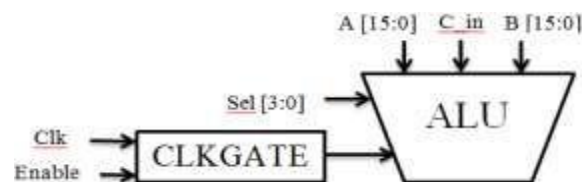


Figure 1 Latch-free Clock Gated ALU design

We use an AND gate in clock gate if clock is active on the rising edge. We use an OR gate in clock gate if clock is active on the falling edge. Using idea given in [4] and [5], we develop following ALU design as shown in Figure1.

3.2. Problem in Latch-Free Clock Gated Design

If enable signal goes inactive in between the clock pulse then gated clock terminated before his life time as shown in Figure 2.

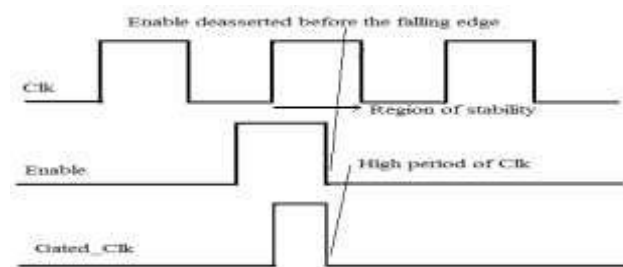


Figure 2 Problem in Latch-Free Clock Gated Design

3.3. Latch Based Clock Gated ALU Design

The latch-based clock gate consists of a level sensitive latch in design to hold the enable signal from the active edge to the inactive edge of the clock as shown in Figure 3.

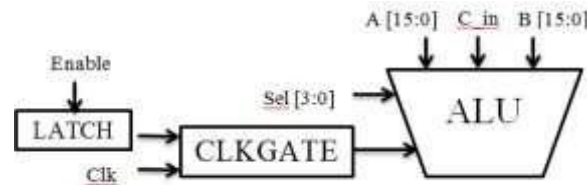


Figure 3 Latch Based Clock Gated ALU Design.

This paper implements the latch free CG for a 16-bit ALU on a Spartan 3E FPGA. The RTL implementation and the power analysis is presented in the paper.

4. LOW-POWER AND AREA-EFFICIENT CARRY SELECT ADDER

For low power consumption ALU, we need an architecture which has an efficient adder for propagation and generation block. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

Carry Select Adder (CSLA) is one of the fastest adders used in many data- processing processors to perform fast arithmetic functions. The CSLA is used in many computational systems to overcome the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA shown in figure 4 is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input $c_{in} = 0$ and $c_{in} = 1$, then the final sum and carry are selected by the multiplexers (mux).

From the regular structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. The proposed design has reduced area and power as compared with the regular CSLA with only a slight increase in the delay.

The basic idea of this proposed structure shown in figure 5 is to use Binary to Excess-1 Converter (BEC) instead of RCA with $c_{in} = 1$ in the regular CSLA to achieve lower area and power consumption [6]-[7]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure of RCA.

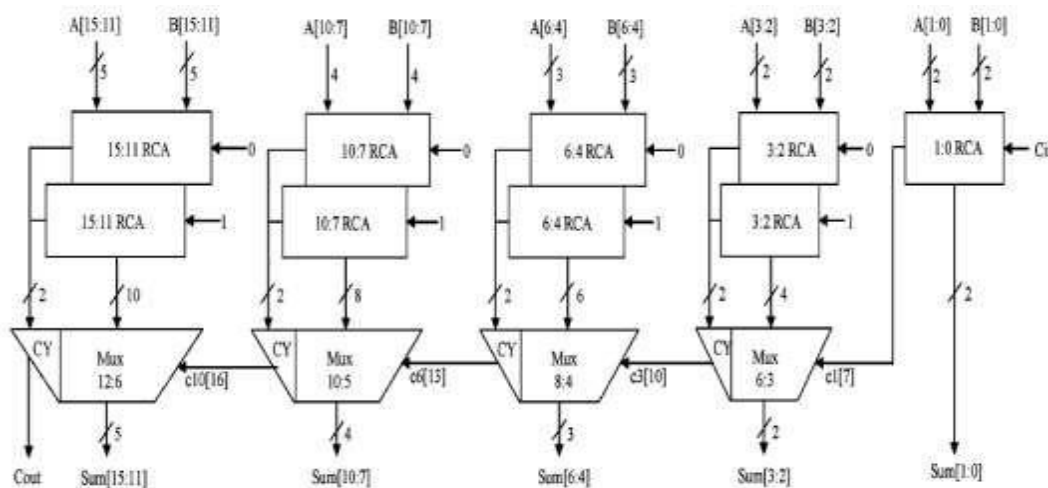


Figure 4 Regular structure of carry select adder.

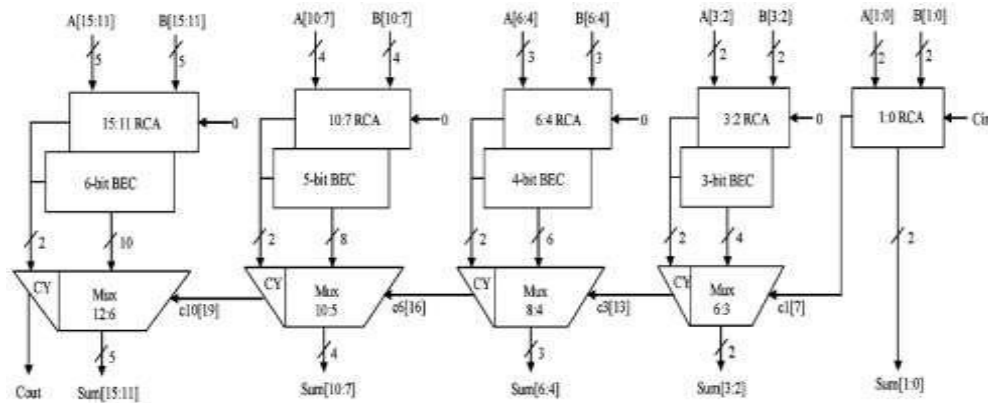


Figure 5 Proposed structure of carry select adder.V.ALU



Figure 6 Conventional ALU.

We have introduced conventional ALU shown in figure 6 to compare the results of proposed ALU shown in figure 8. ALU has 5 inputs. They are A, B, sel, reset and clk. Out returns the result of the ALU operation. A and B are two 16 bit data inputs to ALU. Input sel [3:0] determines which operation of ALU is to be performed based on fetched opcode by instruction decoder. The whole process is carried out based on reset input.

Table 1 Functions of arithmetic and logic unit

Unary	sel	Arithmetic & logic	sel
clear	0000	Adder(carry select adder)	0111
Complement a	0001	Subtraction	1000
Complement b	0010	Add with carry	1001
increment	0011	Subtract with barrow	1010
decrement	0100	Logical and	1011
Left shift	0101	Logical or	1100
Right shift	0110	Logical xor	1101
		Logical xnor	1110
		Logical nand	1111

As listed in the above table 1, there are 16 functions based on 4 bit opcode. The opcode selects the particular arithmetic or logical operations. The first 7 are unary operations and next 9 are arithmetic and logical operations. The ALU generates 3 flags-Zero (Z), Carry (C) and Sign (S). Z-whose result is zero for any operation performed on 16 bit ALU, Carry (C) generates a carry when an addition is performed

on 16 bit or generates a borrow when subtraction is performed on 16 bit data, Sign (S) is generated when the result of any operation is negative.



Figure 7 ALU with clock gating.

Here enable is extra input for generation of clock gate as shown in Figure 7. When clock is high, then clock and en fed to AND gate and when clock is low, then clock and en fed to OR gate. The output of AND/OR gate is gated clock. The operation of proposed model was clearly depicted with the following logic flow chart shown in figure 8.

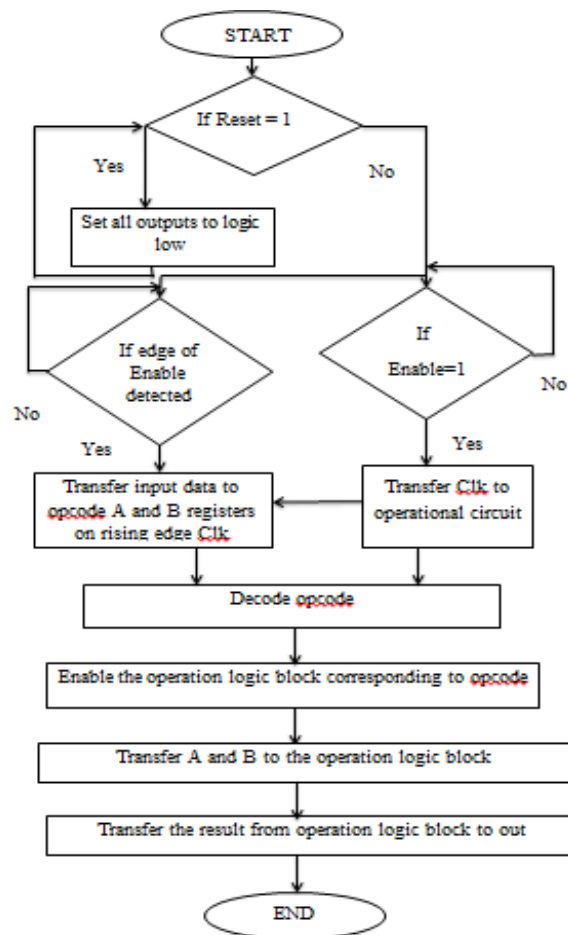


Figure 8: Logic flow chart of proposed model.

In brief how the clock gating plays a role in reduction of power is shown with increment function from conventional to proposed in below figure 9.

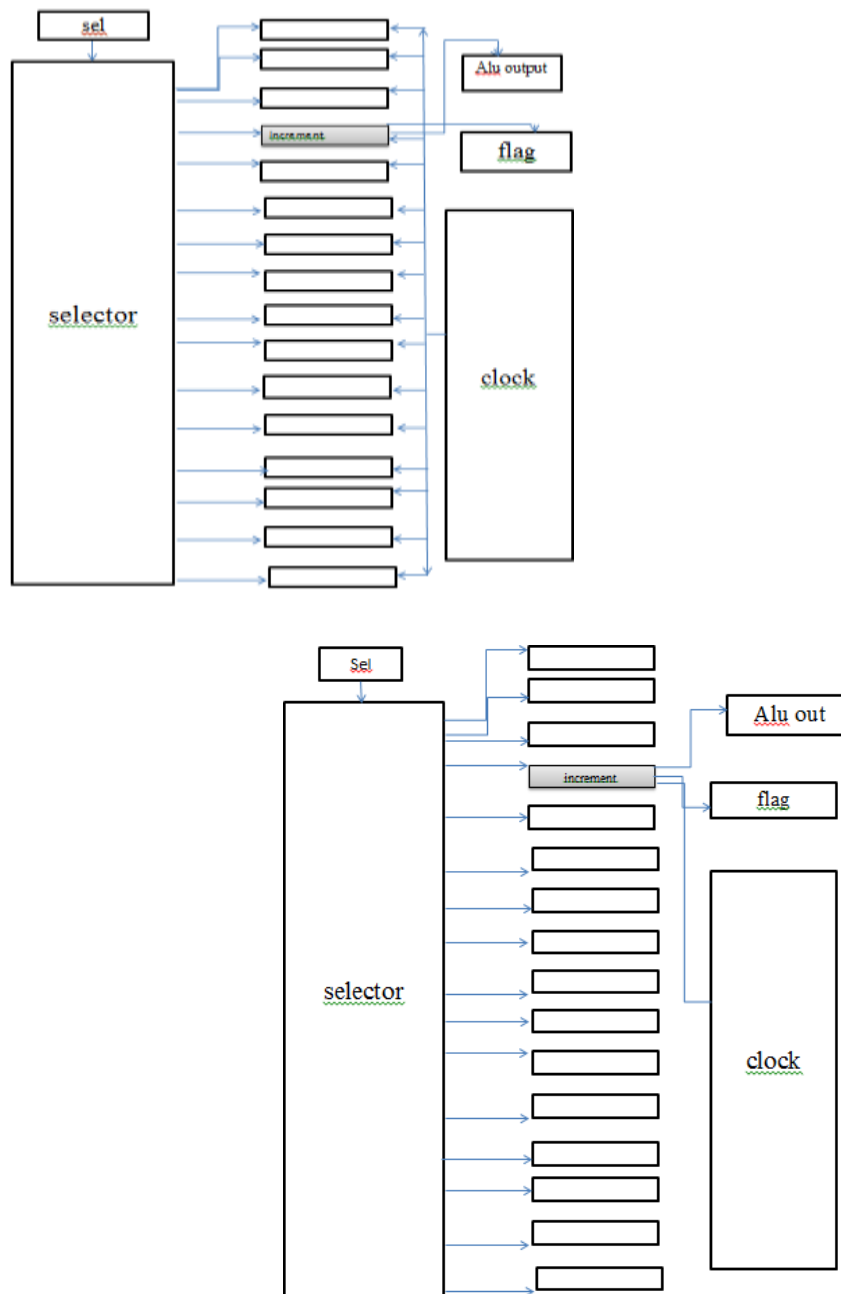
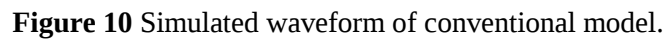


Figure 9 Increment function

5. RESULTS

This section shows simulation and implementation results followed by experimental results of conventional and proposed models. Figure 10 and 11 depicts the timing waveform and RTL schematic of ALU without clock gating. While figure 12 and 13 depicts the timing waveform and RTL schematic of adder implemented in proposed model. There by figure 14 and 15 depicts the timing waveform and RTL schematic of ALU with clock gating.



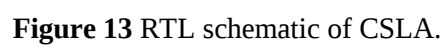
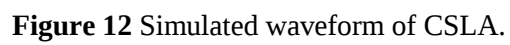




Figure 14 Simulated waveform of proposed model.

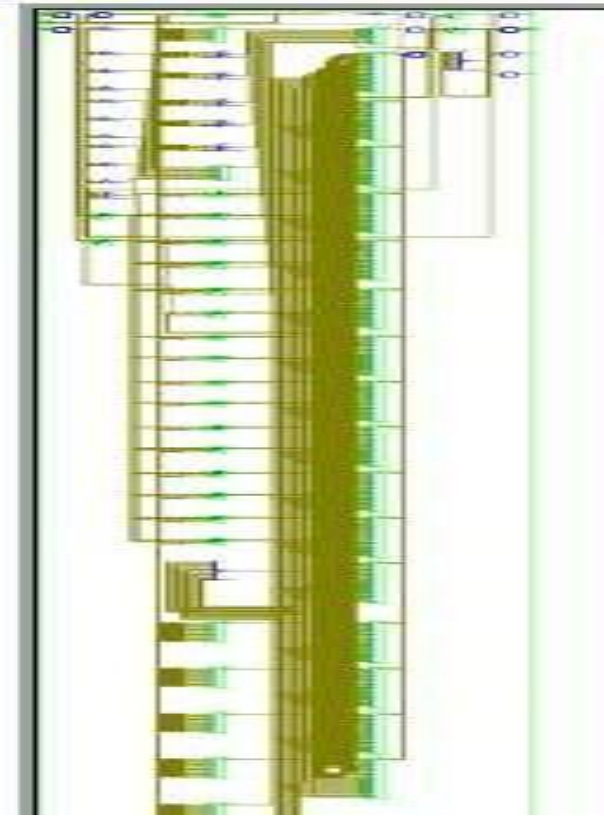


Figure 15 RTL Schematic of proposed model.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	288	4656	6%
Number of Slice Flip Flops	150	9312	1%
Number of 4 input LUTs	518	9312	5%
Number of bonded IOBs	57	232	24%
Number of GCLKs	1	24	4%

Table 2 Device utilization summery of conventional model

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	387	4656	8%
Number of Slice Flip Flops	381	9312	1%
Number of 4-input LUTs	696	9312	7%
Number of bonded IOBs	57	232	24%
Number of GCLKs	1	24	4%

Table 3 Device utilization summary of proposed model

Table 2 and 3 shows the implementation results of both the models using SPARTAN 3E FPGA, realizes that clock gating technique adds the extra hardware to circuit and reduction in power is shown with table 4. it is formulated as

Table 4 Power comparison of both models

Parameter	Conventional model (mW)	Proposed model (mW)
Total power	209	198
Dynamic power	130	119
Quiescent power	79	79

Power reduction % = (number of units gated / Total number of units) × 100 Theoretically expected value is (15/16)*100=93.75% power reduction.

Thus by observation on an average the power reduction is 33% for lower frequency while it is nearly 70% for higher frequencies.

6. CONCLUSION

Finally we have designed above models in VERILOG and simulated with XILINX ISE 12.1 design suit and then implemented using XILINX SPARTAN 3E FPGA and results of both the models are compared. From the results 16 bit ALU with clock gating consumes less power than conventional ALU. Hence it can be concluded that proposed model uses clock gating is a efficient method for reduction in clock and dynamic power by reducing unnecessary switching activities on data and clock buses of unused module while working on current module. This is evidence that how the Power optimization, traditionally relegated to the synthesis, and placement and routing stages, has moved up to the System level and RTL stages.

7. FUTURESCOPE

Clock gating is best technique to reduce dynamic power. In this work, we implemented our design on 90nm Spartan-3E FPGA. Due to scalability in technology, Latest FPGA's like Virtex-7, Kintex-7, Artex-7 based on 28-nm technology contribute significant leakage power consumption. so there is a scope of using this technique in 28nm technology to reduce leakage powers. And here target design is for 16-bit ALU, so there is scope to design this ALU in form of 16-bit or 32-bit or even higher 64-bit.

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