A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design

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ABSTRACT:

The Multiplication is a key fundamental function for many error-tolerant applications. Approximate multiplication is considered to be an efficient technique for trading off energy against performance and accuracy. The proposes an accuracy-controllable multiplier whose final product is generated by a carry maskable adder. The proposed scheme can dynamically select the length of the carry propagation to satisfy the accuracy requirements flexibly. The partial product tree of the multiplier is approximated by the proposed tree compressor. A multiplier design is implemented by employing the carry-maskable adder and the compressor. Compared with a conventional Wallace tree multiplier, the proposed multiplier reduced power consumption depending on the required accuracy. Its silicon area was also smaller. In addition, results from an image processing application demonstrate that the quality of the processed images can be controlled by the proposed multiplier design. Now, we are extended to this project to implement the ROBA (Rounding based approximate multiplier). This is implemented using the rounding nearest value and perform the operation and this also used in the image processing applications

KEYWORDS: ***Approximation, ROBA, Compressors, Error tolerance, Multipliers.***

INTRODUCTION

The crucial part of the arithmetic units are basically built by the multiplier hardware, so multipliers play a prominent role in any design. If we consider a Digital signal processing (DSP) the internal blocks of arithmetic logic designs, where multiplier plays a major role among other operations in the DSP systems. So, in the design of multiplier and accumulate unit (MAC) multipliers play an important role. Next, important design in the MAC unit is the Adder. Adders also share the equal important in this design. By the appropriate function methods different kinds of adders and multipliers designs are been suggested. By the approximate computing the designer can make tradeoffs, accuracy, speed, energy and power consumption.

EXISTING SYSTEM

In applications like multimedia signal processing and data mining which can tolerate error, exact computing units are not always necessary. They can be replaced with their approximate counterparts. Research on approximate computing for error tolerant applications is on the rise. Adders and multipliers form the key components in these applications. In [1], approximate full adders are proposed at transistor level and they are utilized in digital signal processing applications. Their proposed full adders are used in accumulation of partial products in multipliers. To reduce hardware complexity of multipliers, truncation is widely employed in fixed-width multiplier designs. Then a constant or variable correction term is added to compensate for the quantization error introduced by the truncated part [2], [3]. Approximation techniques in multipliers focus on accumulation of partial products, which is crucial in terms of power consumption. Broken array multiplier is implemented in [4], where the least significant bits of inputs are truncated, while forming partial products to reduce hardware complexity.

DISADVANTAGES:

- More Logic complexity
- More power and more delay

PROPOSED SYSTEM

The proposed multiplier in saves few adder circuits in partial product accumulation. In two designs of approximate 4-2 compressors are presented and used in partial product reduction tree of four variants of 8 × 8 Dadda multiplier. The major drawback of the proposed compressors is that they give nonzero output for zero valued inputs, which largely affects the mean relative error (MRE) as discussed later. The approximate design proposed in this brief overcomes the existing drawback. This leads to better precision. In static segment multiplier (SSM) proposed in m-bit segments are derived from n-bit operands based on leading 1 bit of the operands. Then, m × m multiplication is performed instead of n × n multiplication, where m<n. Partial product perforation (PPP) multiplier in omits k successive partial products starting from jth position, where j ∈ [0, n-1] and k ∈ [1, min(n-j, n-1)] of a n-bit multiplier. In 2 × 2 approximate multiplier based on modifying an entry in the Karnaugh map is proposed and used as a building block to construct 4 × 4 and 8 × 8 multipliers. In inaccurate counter design has been proposed for use in power efficient Wallace tree multiplier. A new approximate adder is presented in which is utilized for partial product accumulation of the multiplier. For 16-bit approximate multiplier reduction in power is accomplished compared to exact multiplier. Approximation of 8-bit Wallace tree multiplier due to voltage over-scaling (VOS) is discussed in Lower supply voltage

creates paths failing to meet delay constraints leading to error

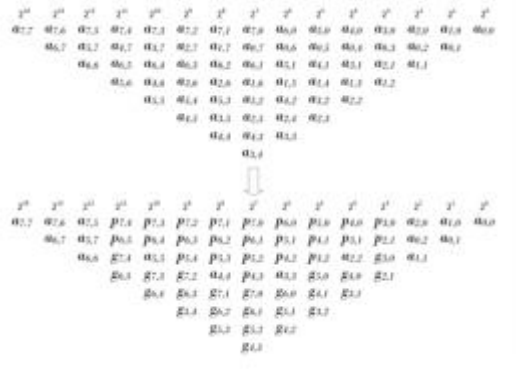

Fig 1: Transformation of generated partial products into altered partial product

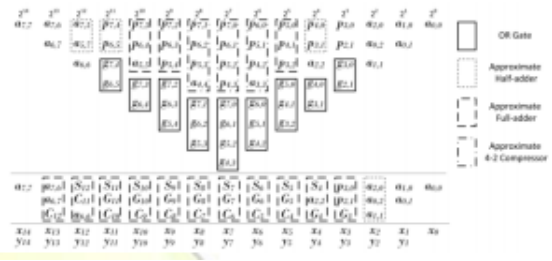

Fig. 2: Reduction of altered partial products.

EXTENSTION

The main idea behind the proposed approximate multipliers to make use of the ease of operation when the numbers are two to the power (2n). To elaborate on the operation of the approximate multiplier, first, let us denote the rounded numbers of the input of A and B by Ar and Br, respectively. The multiplication of A by B may be rewritten as

$$A \times B = (Ar - A) \times (Br - B) + Ar \times B + Br \times A - Ar \times Br.$$

Fig. 2 shows the reduction of altered partial product matrix of 8 × 8 approximate multiplier. It requires two stages to produce sum and carry outputs for vector merge addition step. Four 2-input OR gates, four 3-input OR gates, and one 4-input OR gates are required for the reduction of generate signals from columns 3 to 11. The resultant signals of OR gates are labeled as Gi corresponding to the column i with weight 2i . For reducing other partial products, 3 approximate half-adders, 3 approximate full-adders, and 3 approximate compressors are required in the first stage to produce Sum and Carr y signals, Si and Ci corresponding to column i. The elements in the second stage are reduced using 1 approximate half-adder and 11 approximate full-adders producing final two operands xi and yi to be fed to ripple carry adder for the final computation of the results

The key observation is that the multiplications of Ar ×Br, Ar×B, and Br×A may be implemented just by the shift operation. The hardware implementation of (Ar −A) × (Br −B), however, is rather complex. The weight of this term in the final result, which depends on differences of the exact numbers from their rounded ones, is typically small. Hence, we propose to omit this part from above equation, helping simplify the multiplication operation. Hence, to perform the multiplication process, the following expression is used:

$$A\times B\sim=Ar\times B+Br\times A-Ar\times Br.$$

Thus, one can perform the multiplication operation using three shift and two addition/subtraction operations. In this approach, the nearest values for A and Bin the form of 2n should be determined. When the value of A(or B) is equal to the 3 ×2p−2(where p is an arbitrary positive integer larger than one), it has two nearest values in the form of2nwith equal absolute differences that are 2pand 2p−1. While both values lead to the same effect on the accuracy of the proposed multiplier, selecting the larger one (except for the case of p=2) leads to a smaller hardware implementation for determining the nearest rounded value, and hence, it is considered in this paper. It originates from the fact that the numbers in the form of 3×2p−2are considered as do not care in both rounding up and down simplifying the process, and smaller logic expressions may be achieved if they are used in the rounding up.

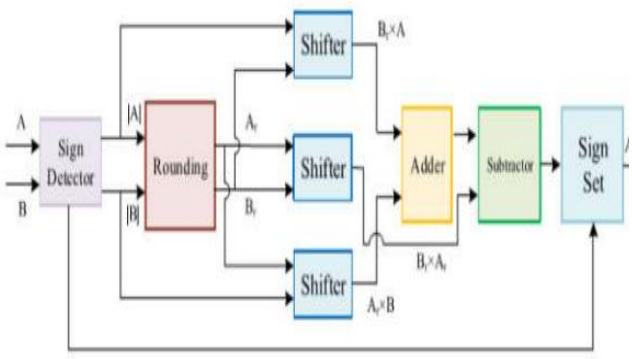

Fig.3: Block diagram for the hardware implementation of the proposed multiplier

CONCLUSION

In this paper we propose a rounding based approximate multiplier (ROBA). By modifying the conventional multiplier for the accurate results. Compared with the conventional multiplier the modified multiplier gives exact result to the given inputs and the multiplier can also perform operations which are not in the form of 2n (as performed in the conventional method) so, the exact result can be obtained for the numbers irrespective of 2n . The ROBA is designed using Xilinx ISE 14.5 and results are shown above and other parameters like area power delay are been calculated using cadence encounter and the design of MAC unit is also implemented in Xilinx ISE 14.5

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