# ASYMMETRICALLY-DRIVEN CURRENT-BASED CHIREIX CLASS-F POWER AMPLIFIER EMBEDDING DEVICE MODEL

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***Abstract*—**
In order to construct an asymmetrically driven class-F Chireix power amplifier, model-based nonlinear embedding is used for the first time (PA). The ideal load impedances for the fundamental and multi-harmonics required at the pack- age reference planes are found using the embedding model of a 15 W GaN HEMT such that the two intrinsic transistors can operate with a previously reported ideal current-based Chireix combin- er. The phase offset of the Chireix combiner is preserved throughout the design from the intrinsic and packaged nodes up to the drive generators by using a symmetric circuit topology. This embedded Chireix PA is discovered to require asymmetrical amplitude and phase modulated input, in contrast to the traditional Chireix PA, which is powered with constant envelope signals.
***Index Terms*—**Chireix, outphasing, power amplifiers

## INTRODUCTION

The Chireix outphasing architechture is one of the most in- triguing techniques for designing high efficiency RF PAs. The original Chireix outphasing architecture consists of two ampli- fiers and one lossless combiner typically implemented using a stub and one quarter wave transmission line in each path [1]. According to the Chireix combiner theory [1], the two ampli- fiers can then be both operated in saturation with constant envelope signals using only phase modulation to ensure a high efficiency operation for a wide range of output power.

Conventional Chireix combiner theory is usually presented using ideal voltage sources for the transistors and thus ne- glects the linear and nonlinear device parasistics between the intrinsic and the packaged reference planes of both transistors [2]. Load-pull technique can then be used to search for the load which compensates for the linear and nonlinear device parasitics such that PAs operate with outphasing [3].

This work relies on a novel current-based Chireix outphasing analysis [4] coupled with a nonlinear embedding model [5], in contrast to the usual Chireix theory. The em- bedding.device model offers direct access to the transistor's inherent current source. Without using a load-pull search technique at the package reference planes, the appropriate intrinsic drain load values can be established directly by building an ideal Chireix PA with the intrinsic transistor IVs. In order to design the Chireix PA as if the intrinsic devices (IV) were directly connected to the Chireix current combiner while simultaneously establishing the extrinsic loads, analysis with the nonlinear embedding model is required. This results in the desired ideal intrinsic Chireix outphasing operation. Utilizing this specific embedding technique.

## I. CURRENT-BASED CHIREIX PA DESIGN USING AN EMBEDDING DEVICE MODEL

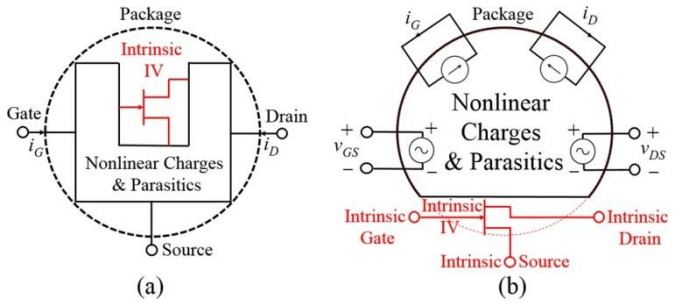


Fig. 1. (a) GaN HEMT device model (b) GaN HEMT *embedding device model* used with the intrinsic and package reference planes revealed.

A GaN HEMT's device model and non-linear embedding model are shown symbolically in Fig. 1, with the FET intrinsic IV indicated in red. When an ideal virtual circuit is created using the FET intrinsic IV, the embedding device model creates the necessary voltages and currents at the package reference planes (red).
Using the embedding model linked to lossless class-F harmonic terminations and a lossless Chireix combiner, Fig. 2 depicts the initial intrinsic design. The lossless network displayed above is virtual at this early design stage, as should be noted. However the final circuit designed will emulate their opera- tion.

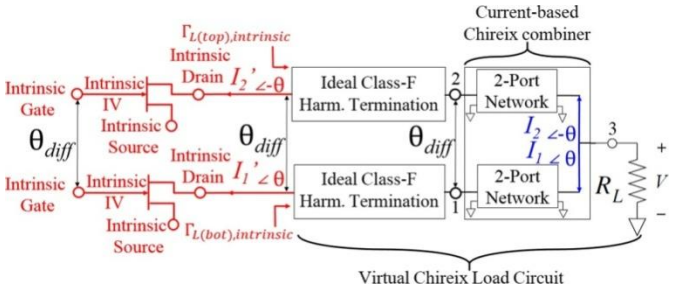


Fig. 2. Two-port current-based Chireix outphasing architecture using the *embedding device model* (red) with the virtual ideal Chireix current combiner and harmonic terminations.

The two lossless 2-port networks are operated with real loads RNIN and RNAS at peak and backoff, respectively, using the analytical expressions presented in [4], and the load currents are utilised to confirm:
$I_1 = I(\theta)[\cos(\theta) + j\sin(\theta)]$, (1)
$I_2 = I(\theta)[\cos(\theta) — j\sin(\theta)]$, (2)
$I_{12} = 2\,I(\theta)\cos(\theta)$. (3)

with the out-phasing angle being 8 degrees. Differential phase is given by diff = — (—) = 2. The combiner delivers the best RNIN to the sources of the drain current when = 0, resulting in the maximum power. The combiner delivers the drain current sources a maximum load RNAS when = O, defined as the outphasing angle of backoff power. The peak-to-average power ratio (PAPR), which is determined by cos-2 (O), follows from (3), leading to:
Note that the same incident power Pinc (θ) is used for the top and bottom transistors at the

intrinsic reference planes.

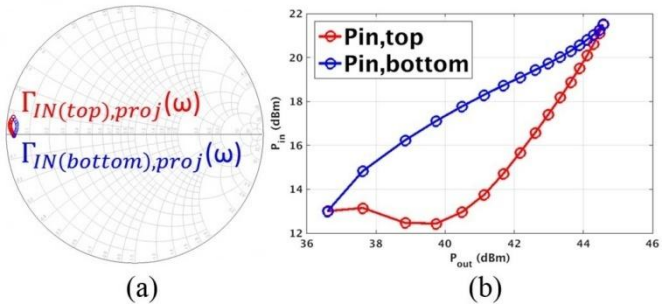


Fig. 3. (a) Asymmetric input reflection coefficient. (b) Asymmetric input power signal.

The non-linear embedding device model's prediction of the asymmetric projected IN() at the package reference planes and the corresponding required input power for the two (top and bottom) transistors are shown in Fig. 3 (a) and (b), respectively. These predictions were made using the targeted line-arly varying intrinsic input signals. It can be seen that throughout the 8dB PAPR output power range, both the projected "IN(")" and the input power are power-dependent. Throughout the 8dB PAPR output power range, the projected input power Pin(top) and Pin(bottom) at the package reference planes are also markedly unequal. As a result, the top and bottom stages at the package reference planes require an asymmetric drive in order to support the desired linearly fluctuating equal-power input signals at the intrinsic reference planes.

We can easily set the ideal input intrinsic voltage signal for driving this ideal load at the chosen outphasing angle based on the structure presented in Figs. 2 and (4). In our design, depending on the chosen 8 dB PAPR and the values of RNIN = 26 Ohm and RNAS = 188 Ohm, ranges from 0 to 66.54 degrees. Due to the non-ideal harmonic terminations and the planned quasi-symmetric Chireix combiner, the final differential phase diff' will vary slightly from the ideal diff.

## II. OUTPHASING CIRCUIT DESIGN

*A. Exact Asymmetric Package Input Signal Design*

The Chireix combiner network is directly derived from the two crucial extreme conditions: peak power ( = 0) and 8dB backoff power ( = O) [4] in order to expedite the design process while keeping the best intrinsic input signals. The ideal outphasing angle for each incident power Pinc() is determined in simulation for power levels between backoff and peak in order to improveefficiency.

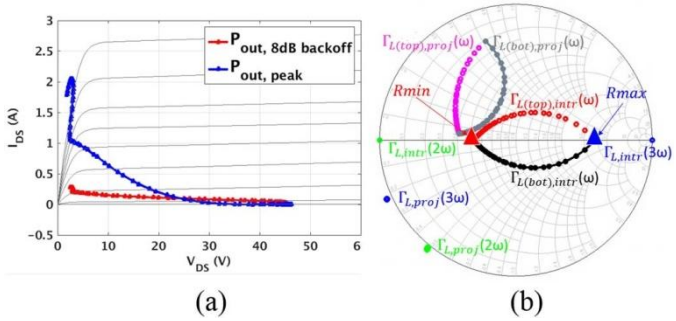


Fig. 4. (a) Plot of the intrinsic load line at peak and 8 dB backoff power.
(b) Plot of the reflection coefficients $\Gamma_L(\omega, 2\omega, 3\omega)$ provided by the Chireix combiner at the intrinsic and package reference planes before and after projec- tion with the embedding model respectively.

After determining the ideal input signals, we now focus on the ideal output loads that the embedding model depicted in Fig. 2 predicts.
The inherent load lines at peak and 8 dB backoff are shown in Fig. 4(a). Fig. 4 (b) displays the load reflection coefficients L(1, 2, 3) at the intrinsic and package drain of both transistors when driven by the extracted optimal input signal.

For class F operation, the intrinsic harmonic reflection coefficients L,intrincic (2, 3) are set to short and open, respectively. The appropriate ideal L(1, 2, 3) at the package reference planes is then exactly produced by the embedding model. The planned "L(2; 3)" can therefore be easily matched by designing lossless harmonic terminations.

With the aid of the optimising tools in ADS, the true harmonic termination is built utilising a micro-strip line-based design. The voltage and current signals from the package drain to ports 1 and 2 are transformed via the harmonic termination network using the ABCD matrix, as shown in Fig. 2. We can easily create a Chireix combiner to satisfy the quasi-lossless and reciprocal criteria [4] because the voltage and current signals are provided at ports 1 and 2. In short, by taking into consideration the linear and nonlinear parasitics, model-based nonlinear embedding substantially helps the Chireix PA design.

## III. CW LSNA & WCDMA DPD MEASUREMENT RESULTS

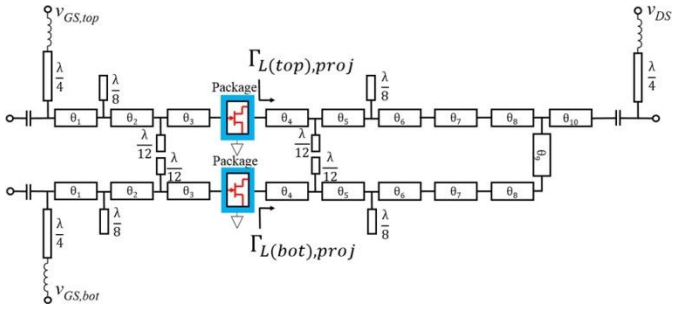


Fig. 5. Schematic of a quasi-symmetric current-based class-F Chireix outphasing power amplifier.

The schematic for the 2 GHz Chireix outphasing PA with 8 dB PAPR is shown in Fig. 5. There were utilised two 15 W GaN HEMTs (CGH27015F). The development of a microstrip line-based quasi-symmetric circuit structure.

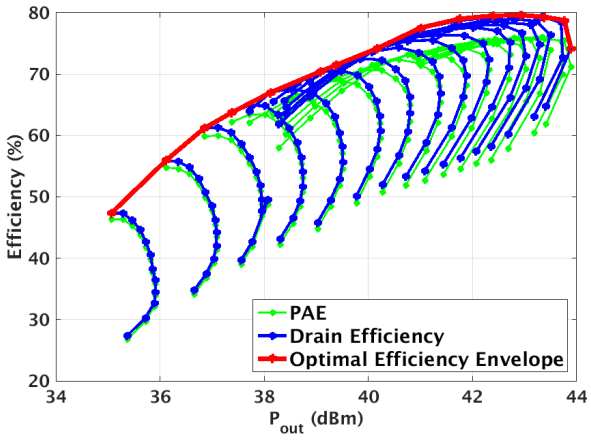


Fig. 6. Asymmetric input power CW measurement at 2 GHz measured with a Large Signal Network Analyzer. The best drain efficiency envelope is shown by the red line. $8_{diff}$ is swept from —40 to —150 degrees. The asym- metric input power ranges from 14.6 to 26.6 dBm.

Using a large signal network analyzer, two-dimensional power and phase sweep CW measurements are displayed in Fig. 6. (LSNA). It should be noted that the asymmetric input signals established in the ADS emCosim are used to drive both transistors. The PAE precisely matches the drain efficiency at backoff since the input matching network is built for the 8 dB backoff power. Figure 6 also displays the typical mixed mode optimal efficiency envelope as a red line. Compared to the conventional pure outphasing mode, it shows a significant increase in efficiency at lower powers [2]. For this mixed mode operation with the 8 dB PAPR range, the efficiency envelope, illustrated in red in Figure 6, maintains the PAE above 55% for virtually the entire range.

The efficiency at the chosen "diff" of the LSNA measurement in Fig. 7 at each power level shows great agreement with the ADS emCosim. Fig. 7 displays the ADS emCosim-simulated complete 360-degree "diff" angle. The "diff" sweeping range for the LSNA measurements was from -150 to - 40 degrees at 8 dB backoff power, producing about 36 dBm of output power with a drain efficiency of 56%. The "diff" produced from simulations and measurements, as shown in Figure 7, is 38.9 and -39.3 degrees, respectively. The "diff" sweeping range was lowered to the range of -150 to -80 degrees in

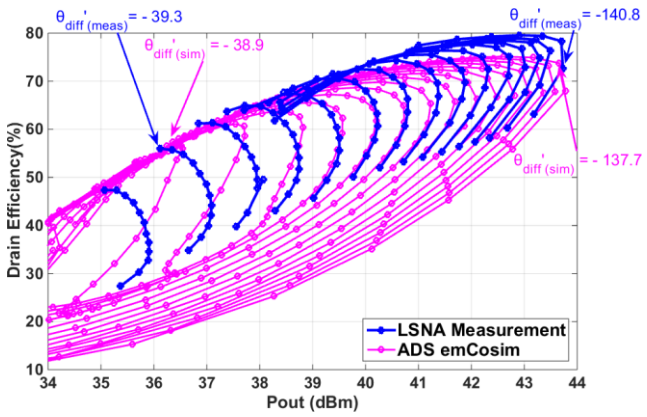

Fig. 7 Comparison between the drain efficiencies obtained from asym- metric input power CW LSNA measurements and ADS emCosim simulations.

order to prevent the GaN transistor from being run at too high temperatures at 44 dBm peak output power. Additionally, Figure 7 demonstrates that, at peak power, the outphasing angle "diff" obtained from simulations and measurements is -137.7 and -140.8 degrees, respectively, with approximately the same drain efficiency of 73 percent.

TABLE I
SUMMARY OF CONCURRENT OUTPHASING PAS

| Tech | Architecture | Freq (MHz) | Signal/ BW (MHz) | η / PAE (Avg) | PAPR (dB) | ACLR (dBc) | Pmax (W) | Ref |
|---|---|---|---|---|---|---|---|---|
| GaN | Chireix | 2300 | W-CDMA/3.84 MHz | 50.5 / 47.0 | 9.6 | -47 | 90 | [2] |
| GaN | 4-input 4-way outphasing[a] | 2140 | W-CDMA/3.84 MHz | 55.6 / - | 9.15 | -33 | 110 | [6] |
| GaN | Broad Band 2-way outphasing | 2300 | W-CDMA/3.84 MHz | 53.5 / - | 9.6 | -49, -56 | 70.6 | [7] |
| LDMOS | RF-in 2-way outphasing | 2170 | W-CDMA/3.84 MHz | 45.8 / 45.4 | 7.5 | -50.2 | 138 | [8] |
| GaN | Embedding Model Chireix | 2000 | W-CDMA/5 MHz | 50[b] / - | 9.3 | -41.5 | 30 | This work |

[a]w/o co-design with PA at device level, [b]with LUT pre-distortion

The DPD test results using a modulated 5 MHz W-CDMA signal are shown in Fig. 8. With 9.3 dB PAPR, a LUT power and phase driver may achieve an average drain efficiency of 50%. After DPD linearization, an ACPR of -41.5 dB can be attained with a marginal improvement in efficiency.

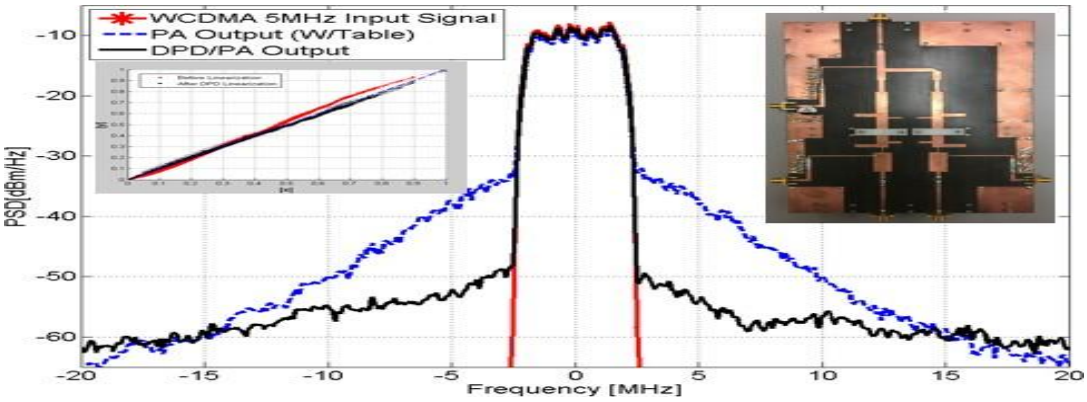


Fig. 8 Modulated signal measurement results before DPD (red), opti- mized LUT drive (blue), and after preliminary DPD (black) with 5 MHz W- CDMA signal at 2 GHz. The AM/AM response is shown in the left inset and the final Chireix PA designed and tested in the right inset.

## IV. CONCLUSIONS

The intrinsic transistor IVs and a recently published current-based Chireix combiner are used to create a virtual Chireix PA first, according to a novel method for creating Chireix PAs. The asymetric input signals and package reference plane impedances necessary to maintain this perfect Chireix intrinsic functioning are then determined by the embedding model. With a 5

MHz W-CDMA signal at 2 GHz, the Chireix PA achieves 79.6 percent peak drain efficiency, 71-77 percent PAE at peak, 55 percent at 8 dB at backoff levels, and above 50 percent average drain efficiency. Broadband outphasing PAs can also be designed using this method of design.

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