PERFORMANCE AND RELIABILITY ANALYSIS FOR VLSI CIRCUITS USING 45NM TECHNOLOGY

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Abstract—
Performance and reliability analysis tests the VLSI circuits over a prolonged period of time at different conditions. Therefore, performance and reliability of an inverter circuit and two CMOS gate interconnect circuit, a combination of two inverters connected with an RC model as an interconnect structure has been analyzed. Reliability in VLSI circuits depends on hot carrier injection, negative biasing temperature instability, positive biasing temperature instability and time-dependent gate oxide breakdown. Reliability is analyzed by comparing power, delay and output voltage. The complete analysis is done using 45nm *gpdk* (generic process design kit) in Cadence Virtuoso

Keywords: **CMOS, HCI, NBTI, PBTI, TDDB**

I. INTRODUCTION

With the advancement in technology device size is shrinking, performance is increased by scaling of transistor size. Thus performance and reliability is becoming a major concern in analyzing the operation of the transistors and circuit. Device characterization in case of temperature variation leads to performance variation thus affecting the device reliability. Reliability of transistors is defined in four terms HCI, NBTI, PBTI and TDDB. Reduction in supply voltage at lower technology results increase in leakage current and electric fields. The most effecting reliability performance parameters are noise margin, leakage current, delay between input-output voltages and reliability in terms of aging. In this paper all these parameters have been analyzed. Performance of transistors affects the drain current and inverted channel [1]. Schematic of basic NMOS, PMOS and Inverter circuit is shown in the Fig1 and Fig2 respectively. Reliability of VLSI interconnects analyzed by HCI, NBTI, PBTI, and TDDB.

HCI affects the reliability of semiconductor of solid state devices. HCI causes increase in threshold voltage and degradation of carrier mobility, especially for NMOS transistors. When the device is biased in strong inversion with large V_{DS}, HCI is a strong voltage dependent factor [2]. **NBTI** is a major aging mechanism which leads to increase in threshold voltage when a negative gate source voltage V_{GS} is applied on the gate of PMOS transistor. It accelerates with high k-dielectrics and metal gate technologies [5]. **TDDB:** Due to low electric field, while utilizing for long time, the gate oxide of MOSFET breaks down, resulting failure of MOSFET. It is a test for constant stress. Cu interconnects are highly affected due to time dependent gate-oxide breakdown of low k-dielectric. Increase in porosity causes decrease in life time. With this issue HCI, NBTI, PBTI leads to reduced I_D, less speed, change in threshold voltage, decrease in trans-conductance, mobility [6].

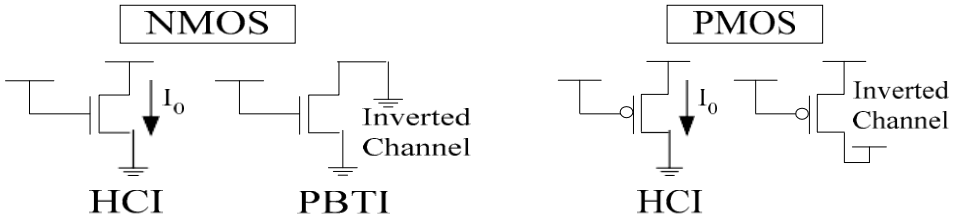


Fig 1. Schematic of NMOS & PMOS circuit

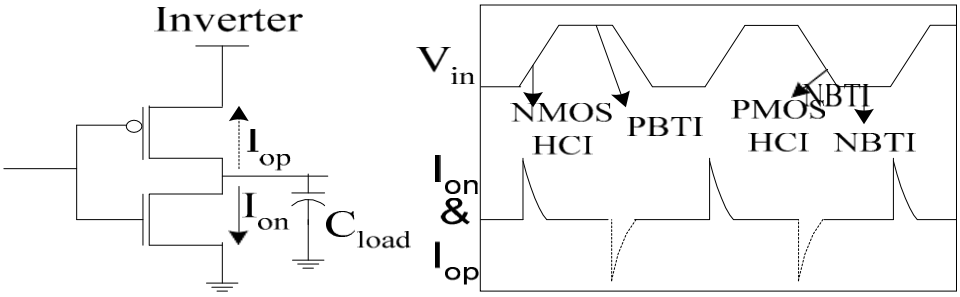
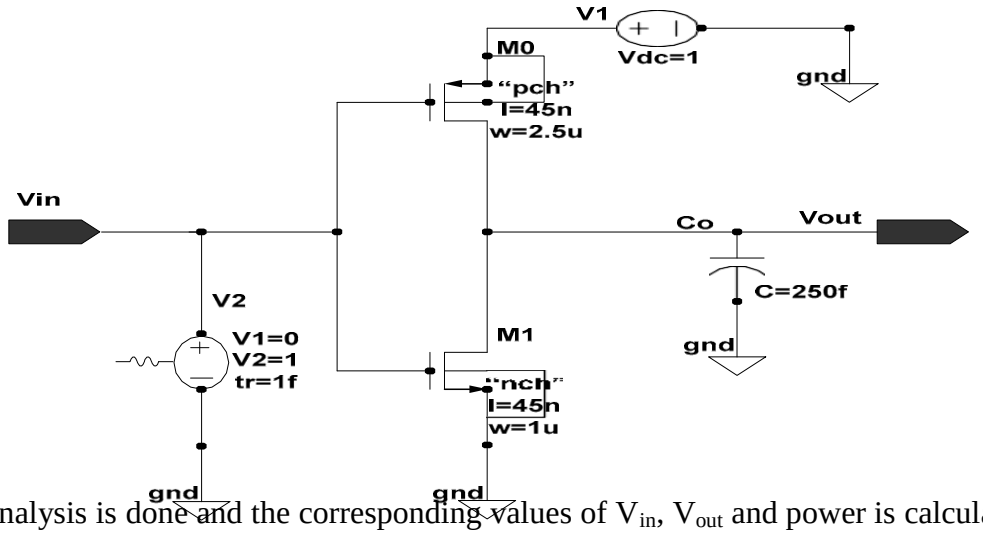


Fig.2. Schematic of Inverter Circuit

PERFORMANCE ANALYSIS OF INVERTER

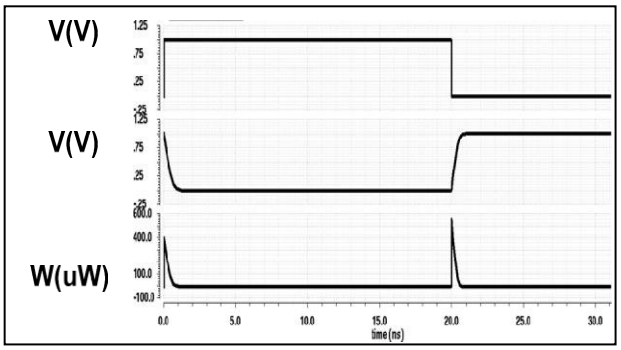
The schematic of an inverter circuit is shown in the Fig.3 which is designed with a PMOS of width 2.5µm, length 45nm, NMOS of width 1µm, length 45nm, using PCH and NCH
increase in temperature. NBTI manifests increase in drain current and trans-conductance of a MOSFET. When NBTI operates with negative gate to source voltage then it affects the devices operating in P-channel [3] [4]. **PBTI** is also a reliability issue in highly scaled CMOS technologies. It is concerned with NMOS transistors. It is a prominent factor in
model libraries respectively. The input is applied using a pulsating signal of 1.1V, rise time of 10ps, fall time 10ps, pulse width 10ns and period of 20ns respectively. The circuit is operated with V_{DC}1.1V using BSIM4 model files, addresses the MOSFET physical effects into sub-100nm regime for 40ns.

Fig.3. Schematic of Inverter



After DC analysis is done and the corresponding values of V_{in}, V_{out} and power is calculated. DC analysis is done in range from -5V to 5V. The evaluated result has been shown in Fig.5.
Transient analysis of inverter is done at 200ns and its simulated waveform is shown in Fig.4

Fig.4. Transient response of Inverter ($V_{in,}$ $V_{out,}$ Power)



Different parameters of the inverter are calculated and shown in Table 1.

Table 1.Values obtained in Transient response of Inverter.

Max Power of Inverter	430.5E-6W	Max Value of Vin	1.1V
Min Power of Inverter	48.1E-11W	Min. Value of Vin	0V
Avg. Power of Inverter	183.5E-8W	Avg. Value of Vin	540.5E-2V
Max. Value of Vout	1.211V	Max Power of PMOS	425E-6W
Min. Value of Vout	-100.3E-2V	Min Power of PMOS	47.3E-17W
Avg. Value of Vout	550.5E-3V	Max Power of NMOS	430.9E-5W
Delay B/w Vin &Vout	11.15E-10S	Min. Power of NMOS	2.05E-15W

Various parameters of inverter are observed on doing DC analysis and is tabulated in the Table 2.
Table 2.Values Obtained at DC analysis of Inverter circuit

Max. Value of Vin	+5V	Min. Value of Vout	41.02E-8V
Min. Value of Vin	-5V	Max. Value of Power	15.45E-5W
Max. Value of Vout	1.1V	Min. Value of Power	17.32E-11W

Noise analysis of inverter is done at frequency 5GHz, amplitude 10dBm.The noise is reduced drastically. Noise ports are added at both terminals and capacitor is placed at load for noise analysis. The schematic for noise analysis of inverter is shown in the Figure 6. The input Capacitor (C0) is of 10f F in series with Port 0.The output Capacitor (C1) is of 10fF and output Capacitor (C2) is of 500fF in parallel with the Port1. signal of 1.1V, rise time of 10ps, fall time 10ps, pulse width 10ns and period of 20ns respectively.

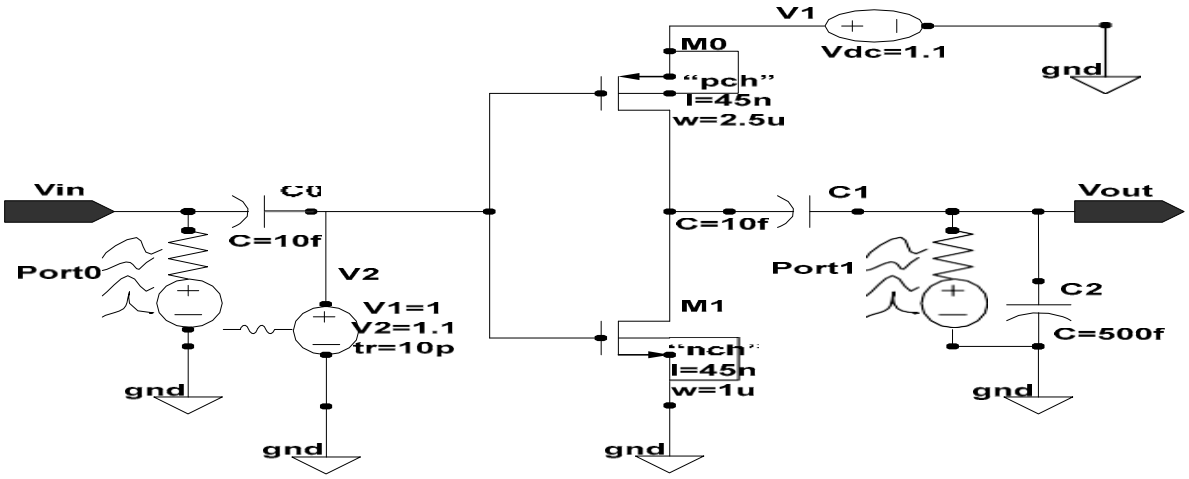


Fig. 6. Schematic of inverter for noise analysis by using ports at both terminals.

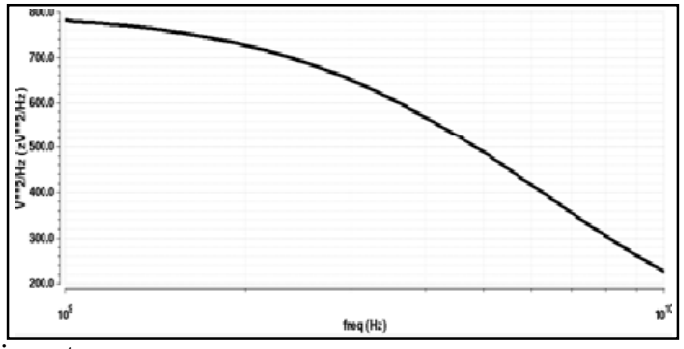


Fig.7. Noise response of inverter

II. RELIABILITY OF INVERTER IN AVERAGE POWER

In conventional terms, reliability is defined as the performance of circuit under different conditions over a prolonged period of time. The reliability of inverter is analyzed at five different intervals. In static DC stress conditions, HCI degrades for both NMOS and PMOS transistors causing variation in threshold voltage, trans-conductance and current driving capability. When the transistors of CMOS circuit are in dynamic operating conditions, the MOSFET terminal voltage varies with time. So we require drain current I_D as function of time. Average power obtained is considered as power delivered by inverter with time period, due to the effect of HCI, NBTI, PBTI & TDDB and circuit failure over certain period of time [6].Reduction in the average power delivered by inverter with time is observed in a test of five years time span. Reliability in terms of average power has been shown in the Fig8.

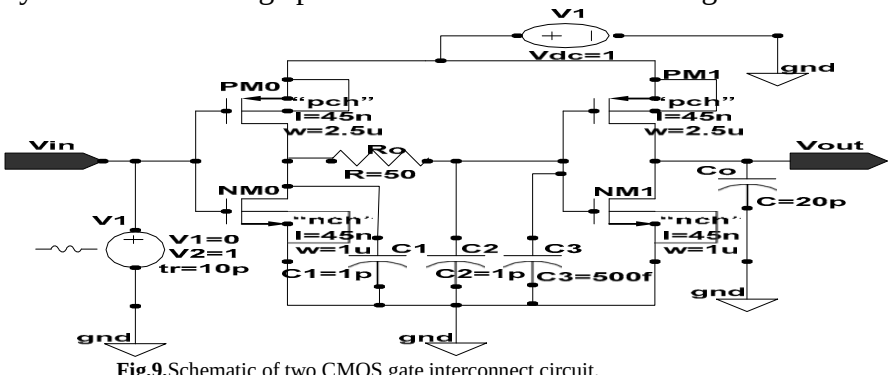


Fig.9. Schematic of two CMOS gate interconnect circuit.

The circuit is operated with VDC 1.1V using BSIM4 model files, addresses the MOSFET physical effects into sub-100nm regime for 40ns. The electrical interconnection between the inverter is composed of an RC model [8]. Table 3 shows various components value in the CMOS gate interconnect circuit. The transient analysis is analyzed for 100ns, and Vin vs Vout is calculated.
Table 3. Passive components used in two CMOS gate interconnect.

R_0	50Ω	C_0	1pF
C_1	1pF	C_2	5pF

Fig10 depicts the transient analysis of the circuit and power consumed by the each transistor, and the tabulated transient analysis results are given in Table 4 respectively.

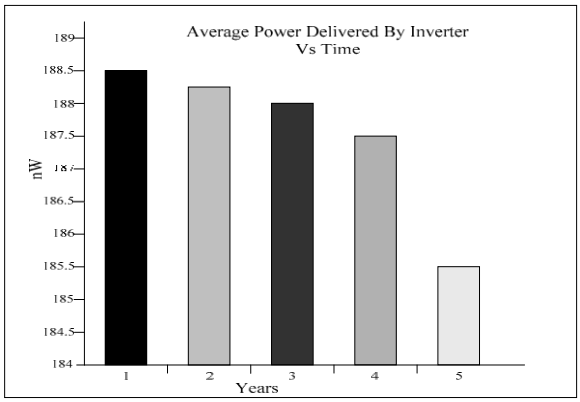


Fig.8. Reliability of inverter in terms of average power delivered and time.

IV.PERFORMANCE ANALYSIS OF TWO CMOS GATE

To estimate the effect of electrical interconnects, a two CMOS gate (a combination of two inverters joined through an RC model) has been implemented. The schematic of two CMOS gate has been shown in Fig9. The schematic of two CMOS gate interconnect circuit. designed contains two PMOS having width of 2.5µm and length 45nm and two NMOS having width of 1µm and length 45nm, using pch and nch model libraries respectively. The input is applied using a pulsating

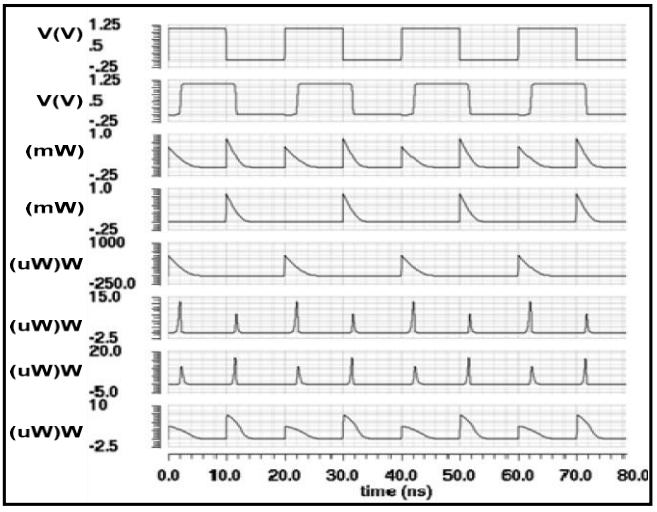


Fig.10. Transient analysis of two CMOS gate interconnect

Table 4. Values obtained in Transient analysis of Two CMOS gate

Max. Value of Vin	1.1V	Min. Power of PMOS-1	30.19E-21W
Min. Value of Vin	0V	Max. Power of NMOS-1	611.0E-6W
Avg. Value of Vin	550.1E-3V	Min. Power of NMOS-1	55.46E-27W
Max. Value of Vout	1.1V	Max. Power of PMOS-2	13.27E-6W
Min. Value of Vout	-157.5E-6V	Min. Power of PMOS-2	390.3E-18W
Avg. Value of Vout	518.9E-3V	Max. Power of NMOS-2	15.98E-6W
Max.Power of Circuit	838.5E-5W	Min. Power of NMOS-2	2.54E-18W
Min. Power of Circuit	114E-12W	Max. Power of R0	7.09E-6W
Avg. Power of Circuit	122.7E-6W	Min. Power of R0	469.2E-21W
Max.Power of PMOS-1	838.9E-6W		

DC analysis is done and V_{in} V_{out} and power is estimated. DC analysis is done in range from -5V to 5V.The result has been shown in Fig11 and Table 5. interconnect for noise analysis. The input capacitor (C_0) is of 1pF in series with Port0, the output capacitor (C_1) is of 1fF and Output capacitor (C_2) is of 5fF in parallel with Port1.The noise response has been shown in the Fig13 estimated to be 780.8E-20.

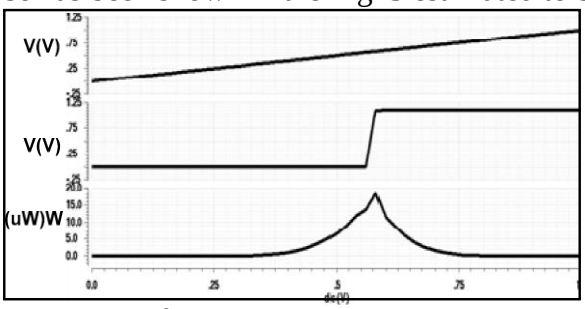


Fig.12.Schematic of Two CMOS gate interconnect noise analysis

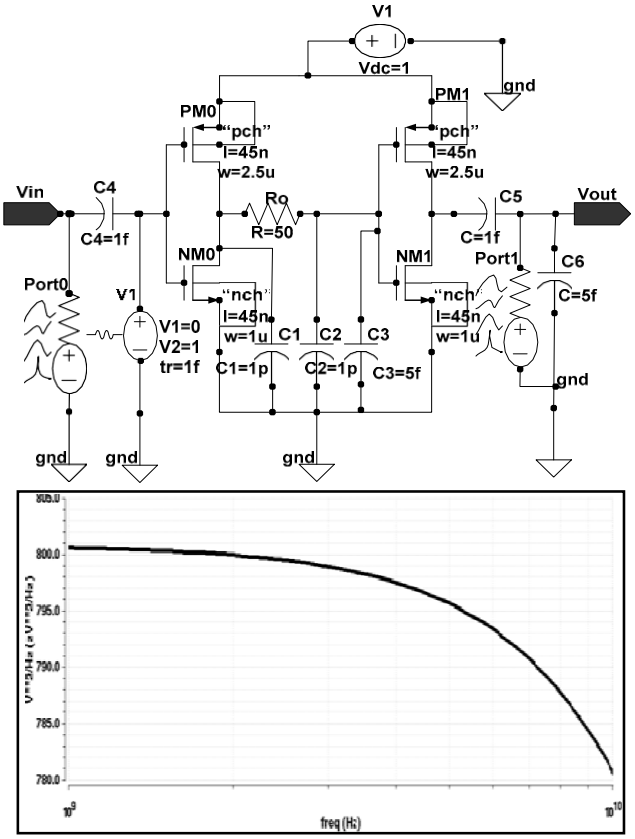


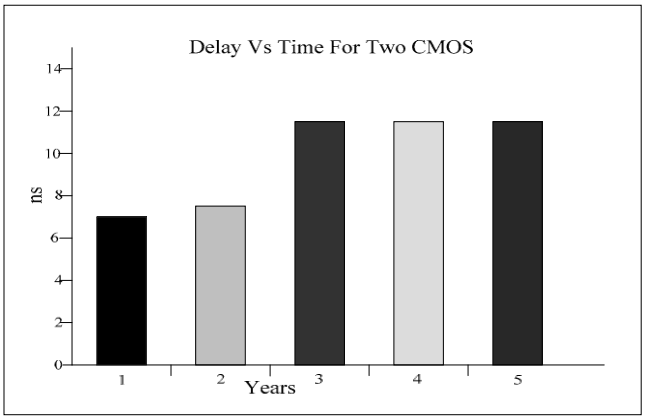
Table 5.Values obtained for DC analysis of Two CMOS gate

Max. Value of Vin	+5V	Max. Value of Power	15.3E-6W
Min. Value of Vin	-5V	Min. Value of Power	81.1E-11W
Max. Value of Vout	1.1V	Avg. Value of Power	1.50E-6W
Min. Value of Vout	38E-8V		

Two CMOS gate interconnect circuit is tested at 5GHz frequency and at an amplitude of 10dBm.The result obtained are acceptable. The noise reduces sharply while inverter starts operating. The Fig12 shows the schematic of Two CMOS gate**Fig.13.** Noise analysis of Two CMOS gate interconnect

III. RELIABILITY EVALUATION OF TWO CMOS GATE INTERCONNECT IN DELAY AND TIME

The reliability analysis is obtained in terms of delay vs time. It is observed that the delay increases with time [8].



\Fig.14. Reliability analysis in terms of delay vs. time of Two CMOS gate interconnect

Reliability analysis has been obtained in terms of average power delivered vs. time for Two CMOS gates interconnect.[9] M.Nourani, and A. R. Attarha, "Detecting Signal-Overshoots for Reliability Analysis in High-Speed System-on-Chips", IEEE Transactions on Reliability, Vol. 51, No. 4, pp. 494-504, 2002.

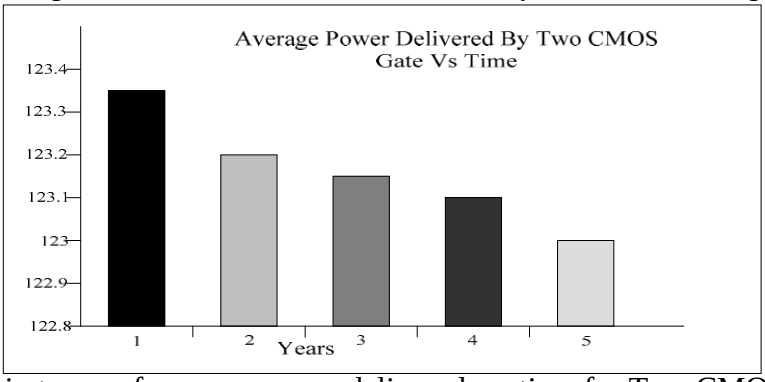


Fig.15. Reliability in terms of average power delivered vs. time for Two CMOS gate interconnect

IV. CONCLUSION

Performance and reliability analysis tests the VLSI circuits over a prolonged period of time at different conditions. Therefore, performance and reliability of an inverter circuit and two CMOS gate interconnect circuit, a combination of two inverters connected with an RC model as an interconnect structure has been analyzed. Reliability in VLSI circuits depends on hot carrier injection, negative biasing temperature instability, positive biasing temperature instability and time-dependent gate oxide breakdown. Reliability is analyzed by comparing power, delay and output voltage. The complete analysis is done using 45nm *gpdk* (generic process design kit) in Cadence Virtuoso

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