VLSI IMPLEMENTATION OF ADC USING ALIASING FREE PULSE WIDTH MODULATION

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***Abstract*—**The Analog to Digital Converters (ADCs) have been in existence for more than 30 years and an integral part of Software Defined Radio, sensor applications and other potential applications. This paper discusses about the implementation of ADC using the Pulse Width Modulation (PWM). The technique of PWM requires a reference signal to be compared with sampled analog input signal to generate Pulse Width Modulated Signals. The main advantage of such ADC is the extension to multiple simultaneous sampling. Application is for building a cheap ADC in a microcontroller based system. These ADCs also feature fast response and low latency, making them ideal for measuring a single input or multiple inputs in biomedical applications.

***Keywords*—** ADC, Pulse Width Modulation, Duty Cycle, Altera Modelsim and ISE, Project Navigator.

I.INTRODUCTION

The Analog to Digital is one of the most inevitable parts of any real time signal processing system where the data is finally processed by computer software like audio [5], and other sensor applications [9]. In this paper a novel architecture of an ADC is presented which based upon the technique of Pulse Width Modulation (PWM) or Pulse Delay Modulation (PDM). The PWM has been widely used in many areas such as Power Electronics [6], Pulse Coded Modulation [1], in controlling the speed of Steep Motors using microcontrollers [2]. It is a very powerful technique where the duty cycle (i.e. ratio of on-period of wave to the total time period of the wave) of a square wave is varied to achieve different functionality in the applications stated above. Medical measurement devices typically require some combination of signal conditioning, including amplifiers, filtering, a reference source and an ADC to resolve the sensor's signal In addition to small size, the analogue circuitry reading the sensor's output should feature low power to provide longer battery life and more readings over time. Small, low-power medical devices powered by a wall socket are also gaining popularity due to the availability of smaller, faster analogue ICs.

There are two different methods of the pulse modulation. One of them is the well established pulse-width modulation (PWM), which is used in many applications, for example, in the switch-mode power supplies (SMPS). PWM wave has a fixed pulse cycle time but its duty cycle vary according to the input signal amplitude. For small input amplitude the pulse width is small, while it is large for large amplitude. Such a signal conversion can be realized by the analog or digital pulse-width modulator (PWM). The second approach for the pulse modulation is to vary the pulse density depending on the input signal amplitude. In this pulse-density modulation (PDM), each sample at the multiplies of the modulator clock rate can be seen as one single pulse. Converting large signal amplidudes results in a high number of samples being at the "high" state, while at small signal amplitudes most samples can be met at the "low" pulse level state. Therefore, this pulse conversion has no fixed cycle time, but can be considered to have a varying pulse frequency.

There are two main types of PWM which result in sampling of the audio signal: naturally sampled PWM (NPWM) and uniformly sampled PWM (UPWM). NPWM is naturally created in the analog PWM modulator, where low power analog audio signal is compared to a carrier (reference) signal. The carrier signal can be a sawtooth or triangle signal, corresponding to single-sided modulation (leading or trailing edge) and doublesided modulation, respectively. In other words, natural sampling is the instantaneous intersection of carrier and signal, and it is used to determine the switching instants of the pulse-modulated pulses. UPWM is typically generated digitally by directly translating an input sample to a pulse width. Further modulation schemes are defined by the switching method which can be a two-level PWM or three-

level PWM. Two-level PWM contains two possible output levels, high and low. Three-level PWM contains three possible output levels since a zero level is included. Class-D amplifiers typically use two-level rather than three-level PWM to control the switching power stage. Three-level PWM is more beneficial because it increases the efficiency of the full-bridge configuration, but at the same time, its control is more complex.

The paper is organized as follows; first the theoretical concepts of an ADC are presented in section II along with the details of the internal circuitry of the proposed ADC. The section III discuss about the modeling in Modelsim and ISE Project Navigator, followed by the discussion of results and graphs in section IV& section V concludes the topic.

II. ANALOG TO DIGITAL CONVERTER

The Analog to Digital Converter (ADC) is a device that converts a time varying continuous analog signal to stream of signal.

The duty cycle of the PWM signal can be computed as ones and zeros so as to process it digitally using a digital computer or a digital signal processor. Almost all ADCs take three inputs namely, the input analog signal, a reference signal and a clock. The block diagram is shown in fig 1.

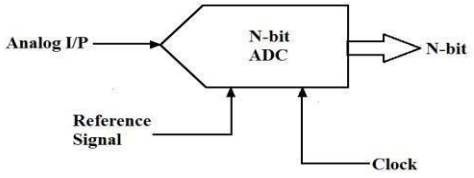


Fig. 1 Basic block diagram of a N-bit ADC

III. IMPLEMENTATION

The ADC proposed in this paper is an 8-bit converter that converts the input analog signal into stream of 8-bits that are generated after every time period Tref of the reference signal.

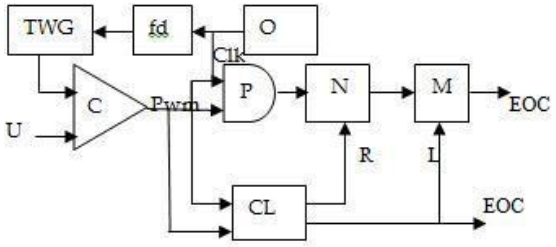


Fig.2 The proposed PWM ADC block diagram

The main idea for this A/D converter is to convert first the input signal into a PWM signal. This can be achieved with a simple comparator and a triangular signal generator as shown in Fig 2.The clock signal coming from the oscillator O is divided with 2n, where n is the number of bits of the converter, with a frequency divider (FD). The divided signal is used to generate the triangular signal (TWG). This is used to be compared with the input signal in order to obtain the PWM signal. As long the input signal is under the triangular one, the output of the comparator is in low state, and it stays in high state if it is above. The PWM signal is the gate signal for, while the clock is on the other input of the AND gate (P). As long as the comparator output is in high state, the clock signal will pass the gate and the counter (N) will count them. At the end of the highs state of the PWM signal the total number of clock periods counted by the counter N represents the conversion result. On the basis of clock and PWM signals, the control logic block (CL) generates two signals: Load signal for storing data in the memory latch (M) and Reset signal for clearing the counter for the next measurement. The "sampling rate" is given by the frequency of the triangle wave

A. Pulse Width Modulation

The Pulse Width Modulation (PWM) is a technique by which the duty ratio of the square wave is varied. According to some logical operation performed on a reference signal and the input signal which generally incorporates amplitude comparison of both signals with respect to each other. As the frequency of the signals vary so does the width. However it should be noted the nature of Pulse Modulated Wave remains constant (and hence the duty cycle of respective pulses) if the frequencies of reference signal and input signal change proportionately with respect to each other. Thus if the ratio of the frequencies of reference signal and input signal remain constant the duty cycle of the pulses in the PWM signal will remain constant. Fig.3 represents one such PWM produced by comparing the amplitude of input signal of 1MHZ with a reference signal of 50MHZ. Hence by means of simple comparison a PWM signal can be generated. Once generated the only task remaining is to encode the varying pulse width to generate suitable digital representation of the input analog signal.

IV. ALIASING FREE PWM

A digital pulse width modulator transforms the amplitude signal a[n] ∈ [0,1] into a train of two-level pulses y[n] of different widths at a fixed pulse period Tp. Hence, the information lying in the amplitude of a[n] is encoded in the widths of the pulses of y[n]. A common PWM method is asymmetric double-edge PWM, where the pulse train y[n] consists of asymmetrical pulses that are centered on the midpoint of the pulse period Tp. The edges of the pulses, the transitions between the two levels 0 and 1, can be determined by finding the intersection points of the amplitude signal a[n] with a triangular reference wave $r[n]$ that is periodic in Tp.

Note that, for the PWM method described here, the amplitude signal a[n] has to fulfill certain constraints. First, the bandwidth of a[n] must be adequately smaller than the reference wave frequency fp = 1/Tp Second, the amplitudes of a[n] have to lie within the interval [0, 1]. In order to use the described asymmetric double-edge PWM for signals that do not meet the latter requirement, appropriate preprocessing steps have to be applied. For a real-valued signal, proper scaling and adding a bias could solve the problem. PWM is performed on the magnitudes of the signal, and phase modulation is performed subsequently. PWM is performed on real and imaginary parts of the signal separately, requiring a signal combiner afterward. Conventional digital asymmetric double edge PWM can be implemented with low computational effort by using a comparator. However, the nonlinear non-band-limited operation of the pulse width modulator inevitably induces aliasing in the resulting pulsed signal y[n]. The aliasing effect causes distortion in and around the frequency band of the amplitude signal a[n]. Hence, when recovering the Amplitude signal a[n] from the pulsed signal y[n], distortion remains within the recovered signal. Due to the aliasing effect, conventional PWM is not suitable for applications where the amplitude signal a[n] has to be recovered with high quality from the pulsed signal y[n],e.g. in burst-mode RF transmitters or digital audio applications. Therefore, the aliasing-free PWM get through aliasing is completely avoided.

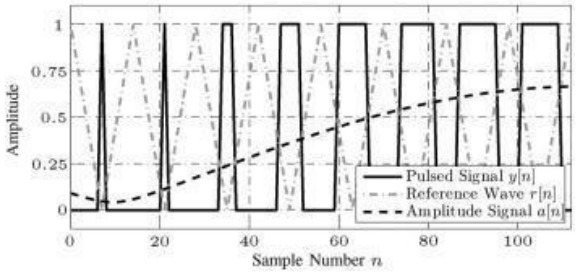


Fig.3 Pulse width modulated signal y[n]

V. MODELING IN MODELSIM ISE PROJECT NAVIGATOR

Modelsim is a user friendly software where complex communication protocols easily which otherwise would be a very difficult task to carry out. Project simulator is an interactive tool for synthesize and implement a design in particular family and a particular device. The following model for the PWM based ADC was designed in Modelsim and Xilinx project simulator to see the output in waveform format and to see the implemented deeply.

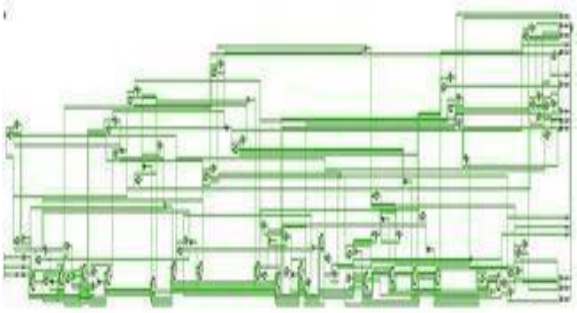


Fig.4 Schematic diagram of aliasing free pwm in ADC

PWM signal then acts as a gate signal to the incoming clock signal having a frequency of 126.9MHz and the final output is fed as a clock signal to a counter which cans maximum count up to 32. Finally the counter is reset after every time period of the reference clock so as to get the digital code for every sample in the PWM signal. So if the pulse width of a particular pulse is higher than the corresponding count value will also be higher and vice versa. In order to reset the count value after every time period of the reference clock a positive edge detector is placed which detects the rising edge of the digitized reference signal.

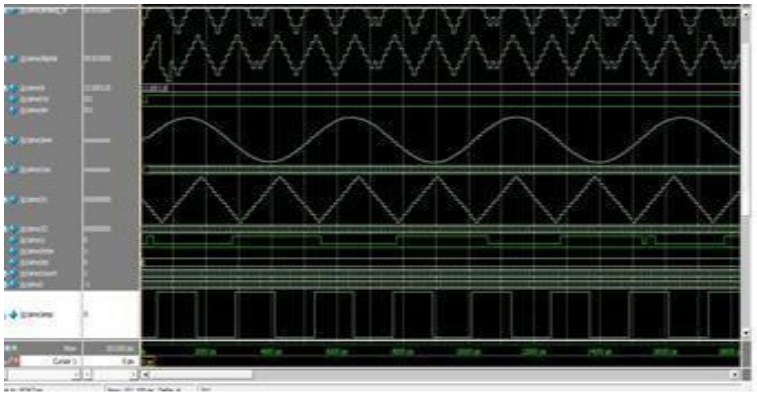


Fig.5 RTL Schematic of AF-PWM based ADC

Hence it can be seen that the final digital output waveform has the shape of the input signal. If we join the peaks of those triangular waveforms then we will exactly get the waveform of the input signal. And hence it can be seen that the input waveform has been finally digitized and converted into digital code.Fig.6 shows the digitized value of the corresponding aliasing free pulse width modulated signal.RTL block diagram of the implemented aliasing free PWM shown in Fig.5 in order to get a clear view of implemented design in target device under the running frequency of 126.9MHZ.

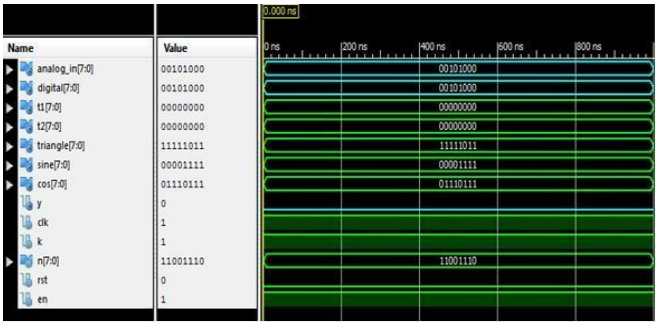


Fig.6 Waveform of aliasing free PWM in ADC

Table I

BLOCK	AREA (cells)	POWER (mW)	DELAY (ns)
PWM based ADC	2.49	0.153	7.880

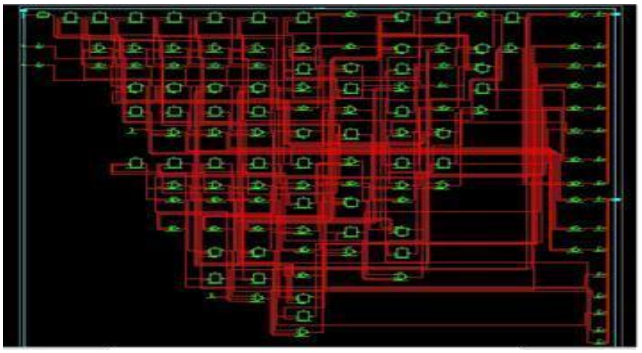


Fig.7.Testbench waveform of AF-PWM based ADC

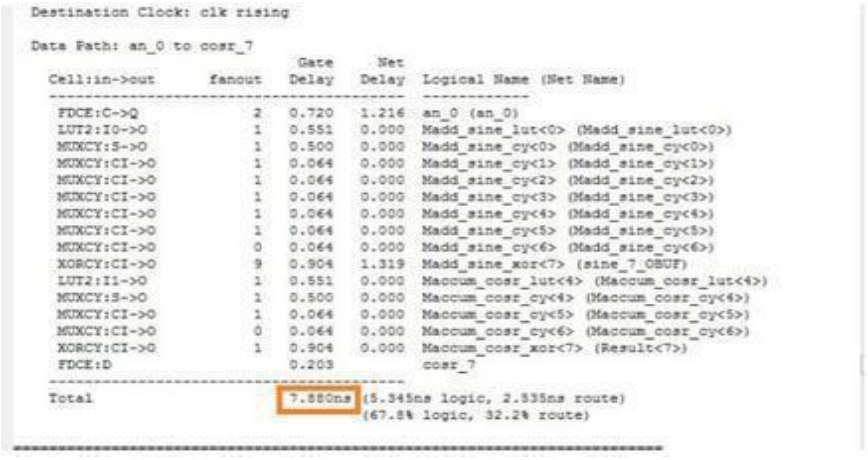
Fig.7.shows the testbench waveform of AF-PWM based ADC. Here the inputs clk=1, rst=0, en=1, k=1,n(7:0)=11001110 are given to the circuit.The digital output is equal to the analog input shows the ADC conversion without quantization error.

Area, Power and Delay of PWM in ADC

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	180	1,536	11%	
Number of 4 input LUTs	179	1,536	11%	
Number of occupied Slices	140	768	18%	
Number of Slices containing only related logic	140	140	100%	
Number of Slices containing unrelated logic	0	140	0%	
Total Number of 4 input LUTs	210	1,536	13%	
Number used as logic	179			
Number used as a route-thru	31			
Number of bonded IOBs	84	124	67%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	2.49			

Fig.8. Area Reports after implementation

Fig.9. Power Reports after implementation



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Destination Clock: clk rising

Data Path: an_0 to cosr_7
                                   Gate     Net
  Cell:in->out      fanout         Delay    Delay   Logical Name (Net Name)
  ----------------------------------------------   ------------
   FDCE:C->Q             2        0.720    1.216   an_0 (an_0)
   LUT2:I0->O            1        0.551    0.000   Madd_sine_lut<0> (Madd_sine_lut<0>)
   MUXCY:S->O            1        0.500    0.000   Madd_sine_cy<0> (Madd_sine_cy<0>)
   MUXCY:CI->O           1        0.064    0.000   Madd_sine_cy<1> (Madd_sine_cy<1>)
   MUXCY:CI->O           1        0.064    0.000   Madd_sine_cy<2> (Madd_sine_cy<2>)
   MUXCY:CI->O           1        0.064    0.000   Madd_sine_cy<3> (Madd_sine_cy<3>)
   MUXCY:CI->O           1        0.064    0.000   Madd_sine_cy<4> (Madd_sine_cy<4>)
   MUXCY:CI->O           1        0.064    0.000   Madd_sine_cy<5> (Madd_sine_cy<5>)
   MUXCY:CI->O           0        0.064    0.000   Madd_sine_cy<6> (Madd_sine_cy<6>)
   XORCY:CI->O           9        0.904    1.319   Madd_sine_xor<7> (sine_7_OBUF)
   LUT2:I1->O            1        0.551    0.000   Maccum_cosr_lut<4> (Maccum_cosr_lut<4>)
   MUXCY:S->O            1        0.500    0.000   Maccum_cosr_cy<4> (Maccum_cosr_cy<4>)
   MUXCY:CI->O           1        0.064    0.000   Maccum_cosr_cy<5> (Maccum_cosr_cy<5>)
   MUXCY:CI->O           0        0.064    0.000   Maccum_cosr_cy<6> (Maccum_cosr_cy<6>)
   XORCY:CI->O           1        0.904    0.000   Maccum_cosr_xor<7> (Result<7>)
   FDCE:D                         0.203            cosr_7
  ----------------------------------------------
  Total                           7.880ns (5.345ns logic, 2.535ns route)
                                          (67.8% logic, 32.2% route)
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Fig.10. Delay Reports after implementation

The performance result has been compared and then it is denoted by table form. The table shows the power consumption, delay and area properties of AF-PWM based ADC. The format of the output clearly represents the concept of Analog to Digital Conversion by using the technique of Pulse Width Modulation (PWM).

VI. CONCLUSION

In this paper a novel architecture for Analog to Digital Converter is presented based on the concepts of Pulse Width Modulation. The A/D conversion uses an intermediary conversion into PWM signal, which can be considered as conversion in quantity time. Each of the PWM states (high or low) carries information about the input signal. Choosing high or low state, the output will be in displaced binary code or respectively in inverted displaced binary code. This architecture does not require any Sample and Hold Circuit and it is relatively faster than other proposed architectures for ADC. The main advantage of such ADC is the extension to multiple simultaneous sampling.

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